An Operating Circuits Design for preventing Electrostatic Discharge in Liquid Crystal Displays

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Abstract

An electrostatic discharge (ESD) or a noise supplied from the outside has an effect on communication between the timing controller (TCON) and the memory element (EEPROM) through the interface between the timing controller and the memory element in liquid crystal displays (LCD). Therefore, we must apply ESD protection methods to LCD operating circuits for a normal operation. Our ESD protection circuit is to prevent from bi-directional communication errors between TCON and EEPROM due to an electrostatic discharge (ESD).

1. Introduction

Electrostatic discharge (ESD) impacts productivity and product reliability in every aspect of today's electronics environment. Electrostatic discharge may upset the normal operation of an electronics system, causing equipment malfunction or failure. Electrostatic discharge damage is also one of the product reliability problems in Liquid Crystal Displays (LCD).

LCD has been applied to many information processing devices which need a display. A LCD panel includes a display unit and a driving circuit unit. In particular, the driving circuit unit includes a timing controller (TCON), which generates the control signal and the data signal, and Electrically Erasable and Programmable Read Only Memory (EEPROM). The TCON and EEPROM are connected by I2C bus. However, electrostatic discharge (ESD) has an effect on communication between TCON and EEPROM through I2C bus. Accordingly, an influence by ESD can deteriorate the image displayed by the display device. Therefore, ESD protection is an important part in side of LCD operating circuits design.

This paper presents a practical method to improve the LCD failure mode preventing from malfunction of TCON due to Electrostatic Discharge (ESD). The abnormal display mechanism, which is generated by ESD, is discussed in Section II. The experimental is described in Section III. Section IV shows the results and discussion. Finally, major conclusions are summarized in Section V.

2. The abnormal display mechanism

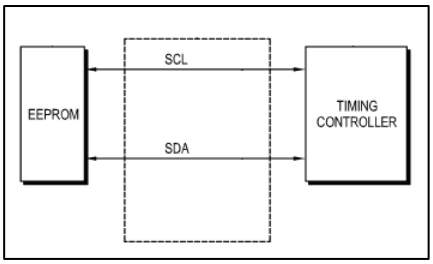


Fig1. Interface between TCON and EEPROM

Fig1 shows the interface between TCON and EEPROM through I2C bus. Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus.

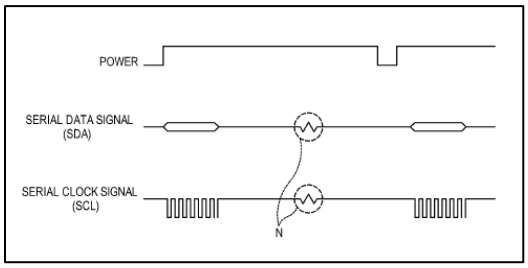


Fig2. Malfunction mechanism by ESD

Fig2 illustrates that ESD generates an unnecessary signal to SCL and SDA. Here, TCON misunderstands

the unnecessary signal as a new start condition and stop condition within the procedure of the I2C bus. In this case, TCON receives again a new display information data from EEPROM. Accordingly, the signal distorted by ESD deteriorates the image displayed by LCD.

3. Experimental

We had to find methods to prevent the distortion of information due to ESD between TCON and EEPROM connected to the I2C bus. Fig3 illustrates conventional circuits and PCB design. Fig4 shows improved circuits and PCB design.

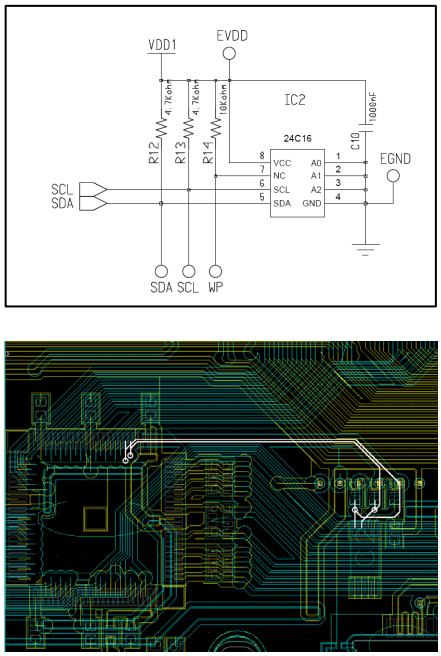
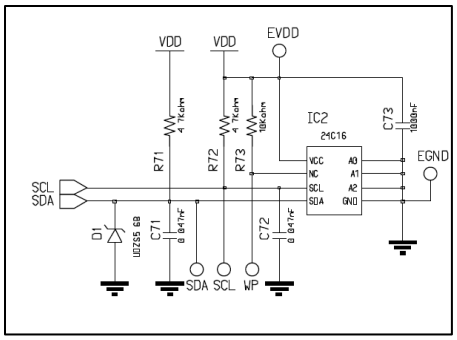


Fig3. Conventional Circuits and PCB design



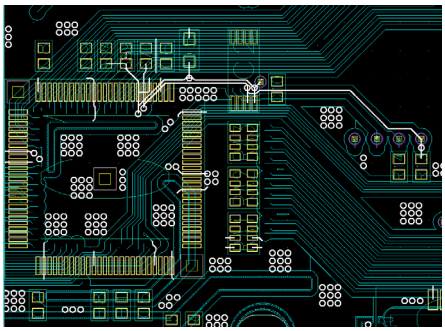


Fig4. Improved Circuits and PCB design

At first, the decoupling caps (47pF) respectively connected to SCL line and SDA line, therefore the electrostatic signal by ESD is diminished not to be recognized by TCON. Accordingly, TCON and EEPROM can be prevented from misunderstanding the electrostatic signal as the new start condition and stop condition of the I2C bus.

Secondly, the zener diode (3.3V) connected to SDA line for maintaining signal without fluctuation of SDA signal when ESD is occurred.

Thirdly, the SCL and SDA signal are supplied with the power from the driving power line. So, the driving power lines independently divided from each other to prevent an unnecessary signal from being generated to SCL and SDA due to ESD.

At last, we changed PCB layout to protect against ESD. So, we arrange EEPROM from TCON within 3mm distance and rewire SCL and SDA. As reducing the distance between TCON and EEPROM, time, which has been effected on by ESD, could be reduced. Accordingly, the electrostatic signal is not to be recognized by TCON and EEPROM.

4. Results

Table1, Fig5 show the ESD test result after applying ESD protection circuits.

Test item	SEC Internal Criteria	
	Test Voltage	Criteria
Air Discharge	±0 ~ ±6KV	OK : Level A [2]
	±6 ~ ±18KV	OK : Level A / Level B [2]
Direct -Infection	±0 ~ ±10KV	OK : Level A / Level B [2]

Note 1) Step
- Firstly Test following voltage spec. , then Test until max. 30kV for limit Test

Note 2) Definition of term
- Level A : Flash noise under 10 times /100 Times is acceptable
- Level B : Self-Recoverable abnormal display and so on
- Level C : System Reset

TEST ITEM	TEST CONDITION	BEFORE			AFTER		
		Sample#1	Sample#2	Sample#3	Sample#1	Sample#2	Sample#3
Contact	±10KV. 150pF / 330Ω, 200 Point, 1 time/Point	50/200, NG	45/200, NG	48/200, NG	0/200, OK	0/200, OK	0/200, OK
Air Discharge 1	±18KV. 150pF / 330Ω, 200 Point, 1 time/Point	45/200, NG	38/200, NG	40/200, NG	0/200, OK	0/200, OK	0/200, OK
Air Discharge 2	±6KV. 150pF / 330Ω, 200 Point, 1 time/Point	15/100, NG	12/100, NG	13/100, NG	0/200, OK	0/200, OK	0/200, OK
CDM	±10KV. 150pF / 330Ω, 200 Point	OK	OK	OK	OK	OK	OK
Input Connector	±2KV. 150pF / 330Ω, 200 Point, Input Con.Pin, 3 time/Point	OK	OK	OK	OK	OK	OK

Table1. ESD Test Criteria and Test Results

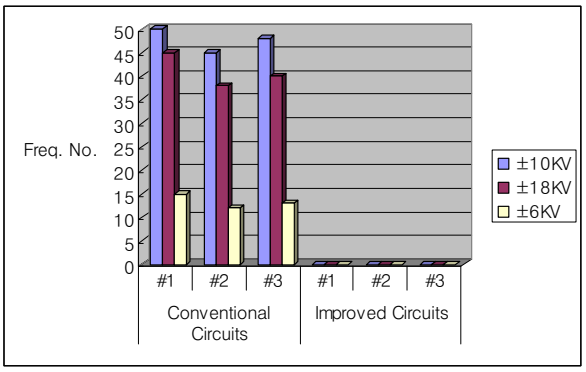


Fig5. The graph of the results

We confirmed that the ESD protection circuit improves the abnormal display due to ESD supplied from the outside through an interface between TCON and EEPROM.

5. Conclusions

In this paper, we present four methods to prevent from bi-directional communication errors between TCON and EEPROM due to ESD.

1. *Connect decoupling caps (47pF) respectively to SCL line and SDA line.*
2. *Connect the zener diode (3.3V) to SDA line.*
3. *Divide driving power lines independently from each other.*
4. *Arrange EEPROM from TCON within 3mm distance and rewire SCL and SDA.*

6. References

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