Polymeric Flexible Field Effect Transistors using Oriented Poly(3-hexylthiophene-2,5-diyl)

Yeong Beom Lee[1] and Hong-Ku Shim[2]
[1]LCD Technology Center, LCD Business, Samsung Electronics Co. Ltd.
Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea, 446-711
TEL:82-31-209-5343, e-mail: yeongbeom.lee@samsung.com
[2]Department of Chemistry, Korea Advanced Institute of Science and Technology, Taejon, Korea 305-701

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Abstract

The properties of oriented poly(3-hexylthiophene-2,5-diyl) in field effect transistors (FETs) have been investigated through mechanical stretching process as the original. Silicon-based FETs shown high mobility of 0.02 cm^2/V s after thermal treatment and 0.0092 cm^2/V s at r.t. PET-based FETs were expected to show a similar performance in mobility to that of silicon-based FETs.

1. Introduction

Organic transistor circuits have been proposed for applications such as low-end display driving circuits and low-cost memory devices for smart cards and price tags. The key building blocks for these circuits are organic thin-film FETs. A thin-film FET consists of materials ranging from conductors and semiconductors, to insulators [1-5].

Many great advantages of processable organic materials can only be realized when combined with compatible fabrication and patterning processes. Conventional photolithography is capable of generating very small feature sizes, but is still relatively expensive for low-end devices.

Highly oriented thin poly(3-hexylthiophene-2,5-diyl) (P3HT) films on polymeric substrate were successfully obtained using the stretching method. The highly oriented P3HT films are used to make a flexible FET. This work is one challenge of the approaches to overcome a performance limit on polymeric transistors and future needs for cheap roll-to-roll process.

2. Experimental

2.1. Instrumentation The P3HT film thickness measured using Tencor Alpha-Step 500 profiler was about 100 nm. Stretching process was performed as the stretching speed of 0.4 mm/min at r.t. and 120 ^oC (under N_2 flow) by universal testing machine (Instrong Co.). The electrical (I-V) characterizations were performed at r.t. using a 4145B Hewlett-Packard semiconductor parameter analyzer and a probe station with optical microscope under dark condition. All measurements were performed at room temperature under ambient atmosphere.

2.2. Materials P3HT, according to literature procedures [6], was purchased from Aldrich Chemical Co., and purified by twice precipitation (methanol and acetone), extraction with chloroform, and column chromatography. Various PET (polyethylene terephtalate) wafers was supported from Saehan Co. in Korea. Anhydrous chloroform (99%+) and 1,1,1,2,3,3-hexamethyl-disilazane (HMDS, 99.9%+) were purchased from Aldrich Chemical Co. and Merck Chemical Co., respectively. The quality of most organic solvents is on semiconducting grade and used without further purification.

2.3. Device Fabrication Purified P3HT (0.02 g) was totally solved in chloroform (1.0 mL) and the solution was filtered through 0.2 micro teflon filter. Two reference silicon-based FET substrates were cleaned through the sonication in chromerge (5 min) and then H_2O (10 min). The substrates were spin-coated with HMDS (for the improvement of surface adhesion) in spin-rate of 3,000 rpm for 60s and then, with the P3HT solution in spin-rate of 1,500 rpm for 60s. Both thin films showed an excellent homogeneous film quality. Silicon-based FETs as reference FET are differentiated to thermally treat one at 100 ^oC for 1hr or to leave the other at r.t. as it is.

Flexible PET substrates were cleaning through the sonication in H_2O (10 min), acetone (30 min), methanol (30 min) and then H_2O (30 min), sequentially. The substrates were spin-coated with

HMDS in spin-rate of 3,000 rpm for 60s and then, with the P3HT solution in spin-rate of 1,500 rpm for 60s. (as the same condition to that of silicon-based FETs) PET-based FETs are prepared to differentiate from thermal treatment, stretching and stretching direction. Stretching process was performed to elongate maximum two-fold length as the stretching speed of 0.4 mm/min at r.t. and 120 ^{o}C (under N_2 flow) by universal testing machine.

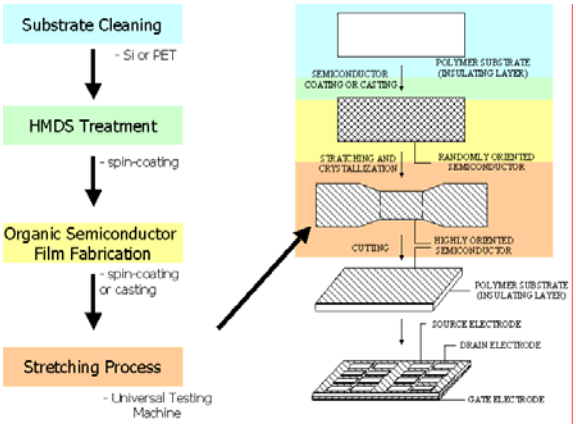

Fig. 1. Manufacturing process of stretched flexible polymeric FETs

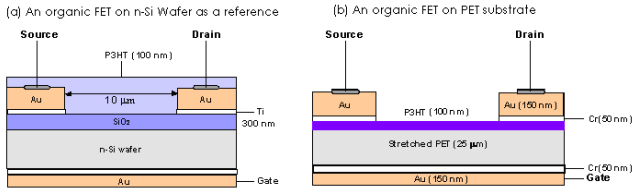

Fig. 2. Polymeric FET configurations

Silicon-based FETs: Briefly, thermally grown silicon dioxide dielectric was grown on n-doped silicon substrate "gates". For the typical "bottom contact" geometry, gold/titanium electrodes forming channels of 100 μm width (W) and 10 μm length (L) were photolithographically defined. The silicon substrates (single crystalline Si wafer substrate coated with developed SiO_2 and vacuum deposited Ti and Au) were prepared by the size of 20 × 20 mm. (Fig. 2(a)) The substrates were cleaning through the sonication in chromerge (5 min) and then H_2O (10 min). The semiconductor (P3HT) was spin-coated over the entire electrode/dielectric surface.

PET-based FETs: 25 μm-thick PET substrates were prepared by the size of 25 × 60 mm. The substrates were cleaning through the sonication in H_2O (10 min), acetone (30 min), methanol (30 min) and then H_2O (30 min), sequentially. (Fig. 2(b)) All substrates were held at room temperature during coating of the semiconductor. For this occasional alternative "top contact" geometry, gold (Au) and chromium (Cr) were defined after semiconductor deposition by using shadow masks with W/L (100/100) = 1 and device area of 20 × 20 mm. All substrates were held at room temperature during deposition. Au electrodes were thermally evaporated onto the semiconducting layer through six regular sandglass-grid array shadow mask to form source and drain contacts and complete the devices. The channels of the transistors were aligned parallel or perpendicular to the stretching direction.

3. Results and discussion

Electrical characteristics of FETs The majority of organic semiconductors exhibit p-type behavior; i.e., the majority carriers are holes (h^+). Their current-voltage (I–V) characteristics can be adequately described by models developed for inorganic semiconductor [7], as shown earlier [3,8,9]. P3HT silicon-based FETs is used here to refer as typical organic FET device characteristics and the methods used to calculate the mobility and I_{on}/I_{off} ratio. Fig. 2 shows two common device configurations used in silicon-based FETs. Fig. 3 shows a typical plot of drain current I_D versus drain voltage V_D at various gate voltages V_G, which corresponds to a device using P3HT as the semiconductor, 3000 Å thick thermally grown silicon dioxide (SiO_2) as the gate insulator, gold/titanium gate, source and drain electrodes. When the gate electrode is biased negatively with respect to the grounded source electrode, P3HT insulated-gate field-effect transistors (IGFETs) operate in the accumulation mode and the accumulated charges are holes. At low V_D, I_D increases linearly with V_D (linear regime) and is approximately determined from the following equation:

$$I_D = \frac{WC_i}{L}\mu\left(V_G - V_T - \frac{V_D}{2}\right)V_D \quad (1)$$

where L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, and m is the field-effect mobility. The latter can be calculated in the linear regime from the transconductance,

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D=const} = \frac{WC_i}{L}\mu V_D \quad (2)$$

by plotting I_D versus V_G at a constant low V_D and equating the value of the slope of this plot to g_m . Fig. 3(b), which corresponds to Fig. 3(a), shows such a

plot, and the calculated mobility value is 0.0092 cm^2/V s at V_D = 60 V. The value of V_D is chosen so that it lies in the linear part of the I_D versus V_D curve. For this device, L was equal to 10 μm and W was equal to 100 μm. Other devices from the same substrate produced field-effect mobility ranging from 0.004 to 0.009 cm^2/Vs.

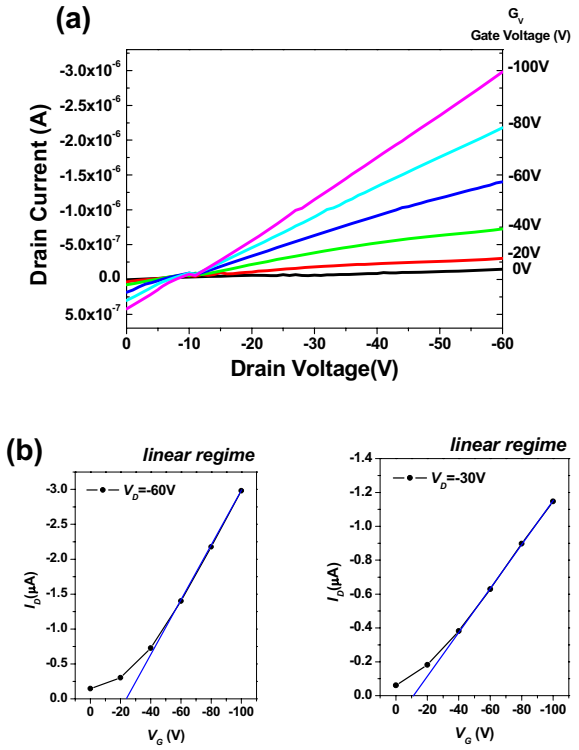

Fig. 3. I-V characteristics of silicon-based P3HT FET device

When the gate electrode is biased positively, P3HT IGFETs operate in the depletion mode, and the channel region is depleted of carriers. I didn't measure the current modulation (the ratio of the current in the accumulation mode over the current in the depletion mode, also referred to as I_{on}/I_{off}) for the device. For V_D more negative than V_G, I_D tends to saturate (saturation regime) owing to the pinch-off of the accumulation layer, and is modeled by the equation,

$$I_D = \frac{WC_i}{2L}\mu\left(V_G - V_T\right)^2 \quad (3)$$

In the saturation regime, μ can be calculated from the slope of the plot of $|I_D|^{1/2}$ versus V_G . For the other device as in Fig. 4, the mobility calculated in the saturation regime was 0.02 cm^2/V s.

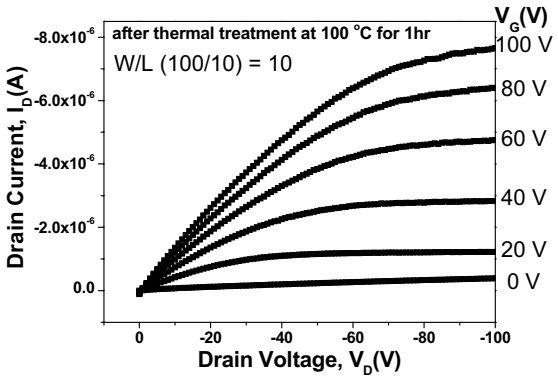

Fig. 4. I-V characteristics of silicon-based P3HT FET device, after thermal treatment

We have a failure to lithograph in PET-based P3HT substrate using photoresist process. Pristine PET substrates were sustained as the originals, but stretched PET substrates were irregularly transformed after PEB at 120 °C for ca. 1 min.

PET-based FET also exhibits p-type semiconductor characteristics. It corresponds to a device with channel length L = 100 μm and width W = 100 μm, and utilizing P3HT as the semiconductor, 25-μm-thick PET as the gate insulator, Cr/Au as the gate electrode, and gold source and drain electrodes.

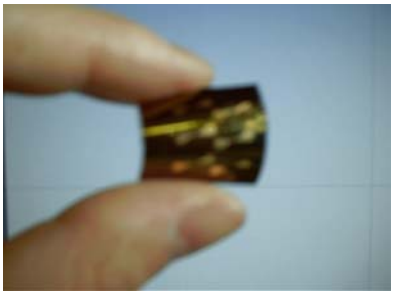

Fig. 5. Flexible PET-based P3HT FETs.

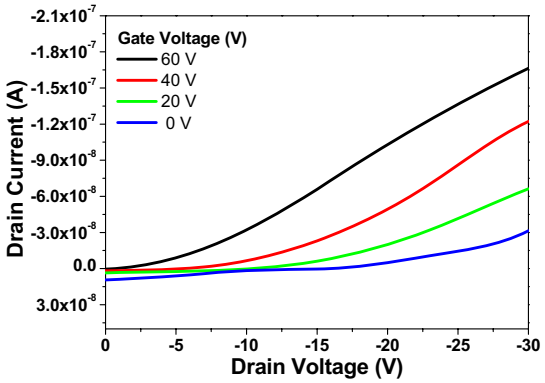

Fig. 6. I-V characteristics of PET-based P3HT FET.

The field-effect mobility μ is expected to be ca. 10^{-3} cm^2/Vs. The measured mobility value is not compared with reported hole mobility from silicon-based IGFETs. It is important that W/L be close to 10 or higher in order to minimize the effects of such currents; otherwise, the mobility is overestimated. An alternative way to achieve this would be to pattern the semiconductor so that its width does not exceed the width of the channel.

The difference can often be observed in mobility values calculated in the linear region and the saturation region. The linear region mobility can be affected by contact problems, and in such cases there are departures from the linearity of the I_D versus V_D curve, which can lead to underestimation of mobility. In the saturation regime, when channel lengths are comparable to the gate insulator thickness or only a few times greater than that thickness, the I_D versus V_D curves do not saturate and exhibit an upward trend at high V_D. Calculating the mobility in the saturation region from such devices can lead to erroneously high values.

4. Summary

The properties of oriented poly(3-hexylthiophene-2,5-diyl) in FETs have been investigated through mechanical stretching process as the original. Silicon-based P3HT FETs with whether or not thermal treatment (at 100 ^oC for 1hr) shown high mobility of 0.02 cm^2/V s and 0.0092 cm^2/V s, respectively. The field-effect mobility was expected to be over 10^{-3} cm^2/V s as similar performance to that of silicon-based P3HT FETs. The stretching process could be used to the application of all polymeric active materials for the roll-to-roll process.

5. References

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