# A Driving Method for Large-Size AMOLED Displays Using a-Si:H TFTs

***Ung-Gyu Min*, Hai-Jung In and Oh-Kyong Kwon***
**Division of Electrical and Computer Engineering, Hanyang University,**
**Haengdang-Dong, Seongdong-Gu, Seoul, 133-791, Korea**
*TEL:82-2-2290-0359, e-mail: minungyu@hotmail.com,okwon@hanyang.ac.kr*

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## Abstract

*A voltage-programming pixel circuit, which compensates the threshold voltage shift of TFTs and the degradation of OLED, is proposed for large sized a-Si:H active matrix organic light emitting diode (AMOLED) applications. Considering threshold voltage variation (or shift), OLED degradation and reverse bias annealing, HSPICE simulation results indicate that luminance error of every gray level is less than 0.4 LSB under the condition of +1V threshold voltage shift and from -0.2 LSB to 2.6 LSB within 30% degradation of OLED in the case of 40-inch full HDTV condition.*

## 1. Introduction

Although many numbers of a-Si:H TFT pixel circuits have been reported for active matrix OLED displays [1-4], there are still lots of issues related to threshold-voltage shift, OLED degradation, and IR-drop on the pixel power buses for realizing AMOLED displays.

Most of the voltage programming pixel structures [1, 2] require additional TFTs to compensate OLED current variation due to the deviation of electrical characteristics of pixel driving TFTs, so the pixel circuit and timing diagram become more complicated, and aperture ratio and panel yield decrease. Current-programming pixel structures [3, 4] can hardly charge the data line to a target voltage with the given small amount of current for a given short row line time in low gray levels. Especially, this issue becomes more severe situation in large-size and high-resolution displays. As the panel size increases, the effectively available programming time gets shorter because RC-delay of scan and data lines increases.

To solve these problems we propose a voltage-programmed pixel circuit, which senses the threshold voltage of the driving TFTs and OLED degradation, compensates them, and suppresses the threshold voltage shift of the driving TFTs by the negative bias annealing during dark-frame-insertion period.

## 2. Proposed pixel structure

Fig. 1 shows the schematic diagram of the proposed driving and pixel circuits. The operating sequence of the driving and pixel circuits is depicted in Fig. 2. The operation is composed of one turn-on-time phase and consecutive frames which consists of D (emission phase) and DFI (dark frame insertion), and there are two types of DFIs. One is for threshold voltage sensing and the other is for negative bias annealing.

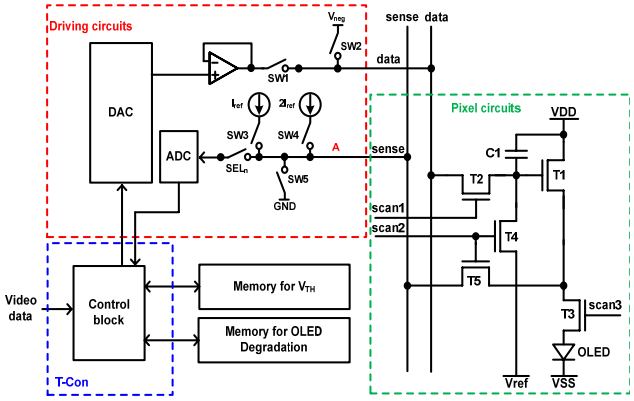


**Fig. 1. Schematic diagram of proposed driving and pixel circuits.**

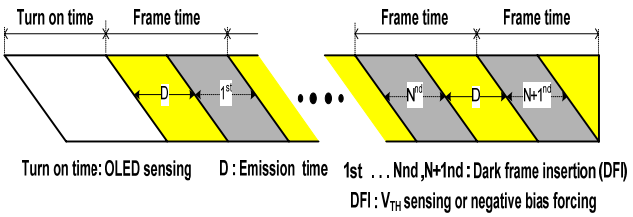


**Fig. 2. Timing diagram of proposed pixel circuits.**

For the new compensation technology presented in this paper, the basic equation for the compensation is given by

$$\frac{100}{\alpha}\times\frac{data}{2^n-1}\times I_{MAX}=\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{G,data}-V_{S,data}-V_{th})^2 \quad (1)$$

where $\alpha$ is the efficiency ratio of OLED with and without degradation in percentile, $n$ is the number of color depth of video data signal, $I_{MAX}$ is the required current for maximum gray level. $\mu$ is the mobility of driving TFT, $C_{ox}$ is the gate capacitance per unit area of the driving TFT, ($W/L$) is width and length radio of the driving TFT, $V_{G,data}$ is the gate voltage of the driving TFT, $V_{S,data}$ is source voltage of the driving TFT, $V_{th}$ is the threshold voltage of the driving TFT. Then, $V_{G,data}$ can be expressed as

$$V_{G,data}=\sqrt{\frac{100}{\alpha}}\times\sqrt{\frac{data}{2^n-1}}\times\sqrt{\frac{2I_{MAX}}{\mu C_{ox}}\times\frac{L}{W}}+V_{S,data}+V_{th}. \quad (2)$$

In equation (2), $\alpha$ factor can be determined during the turn-on-time phase by sensing the anode voltage of OLED and threshold voltage can be sensed in DFI time. $V_{S,data}$ is determined as

$$V_{S,data}=V_{T3,DS,data}+\Delta V_{OLED}+V_{OLED,data}+VSS. \quad (3)$$

In equation (3), $V_{T3,DS,data}$ and $V_{OLED,data}$ are determined by look-up table. $\Delta V_{OLED}$ is determined in turn-on-time phase as shown in Fig. 2. The mobility of a-Si:H is generally uniform across the glass, so $\mu$ can be predicted as the mobility of driving TFTs in panel.

In turn-on-time phase as shown in Fig. 3 (a), in order to determine the degradation of OLED, we connect the SW3 and SW4 sequentially through OLED to read out $\Delta V_{OLED}$, which is used for the input of look-up table to generate $\alpha$ as depicted in Fig. 4. The reason of sequentially connecting two current sources, $I_{REF}$ and $2I_{REF}$, is to eliminate the resistance of T3, T4, and load line. In such a way, we can generate $\Delta V_{OLED}$ and $\alpha$ factor to be stored in the memory for whole panel for OLED compensation.

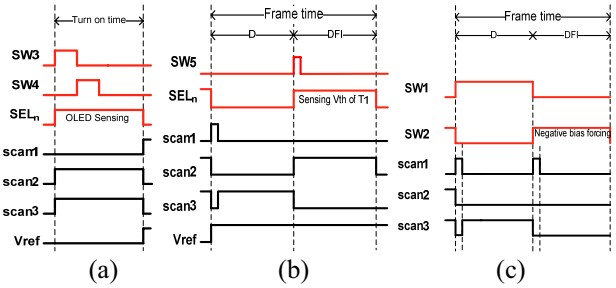


**Fig. 3. The timing diagram of (a) turn on time, (b) frame time with threshold voltage sensing and (c) frame time with negative bias annealing.**

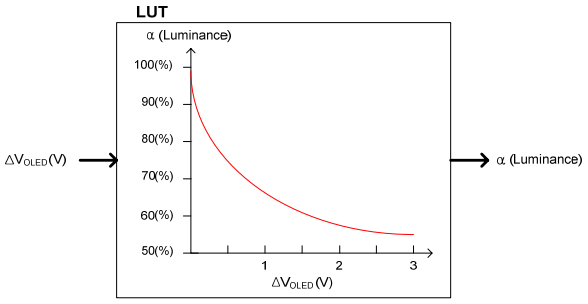


**Fig. 4. Look-up table for $\alpha$**

By adopting DFIs, we can implement 120Hz frame frequency in panel, which can reduce the effect of image burring which exists in hold type displays. At the same time, by taking advantage of the DFI period, we can sense the threshold voltage of driving TFT and force negative bias at the gate of driving TFT to suppress the threshold voltage shift.

For sensing the threshold voltage, $V_{REF}$ is applied at the gate of driving TFT, T1, by turning on T4 and after disconnecting node A from GND by turning off SW5, for frame time, which is 8.3 msec in this paper. The voltage of node A, $V_A$, can be defined as

$$V_A=V_{REF}-V_{th,T1}. \quad (4)$$

In equation (4), $V_{th,T1}$ is the threshold voltage of driving TFT, T1, which is to be stored in memory. To compensate the shift of the threshold voltages of all the driving TFTs, the threshold voltages of whole panel are to be stored in memory periodically. Basically, because the pixels in only one row line per one frame are sensed, to sense all the pixels in panel, we need as many numbers of frames as the number of row line of the panel. The timing diagram of threshold

voltage sensing is presented in Fig. 3 (b).

The timing diagram of negative bias annealing is depicted in Fig. 3 (c). To apply negative bias to the gate of driving TFT during DFI, after sensing threshold voltage of whole panel, we connect $V_{NEG}$ with the gate of T1 by turning on SW2 and T2, while T3, T4, and T5 turn off.

After completion of $V_{th}$ and OLED degradation sensing, the emission current equation of T1 can be expressed as equation (5) by inserting equation (2) and (3) into the saturation current equation of the driving TFT.

$$\begin{aligned} I_{T1,data} &= \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2 \\ &= \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{G,data}-V_{S,data}-V_{th})^2 . \\ &= \frac{100}{\alpha}\times\frac{data}{2^n-1}\times I_{MAX} \end{aligned} \quad (5)$$

Equation (5) shows that the emission current does not depend on threshold voltage of driving TFTs.

## 3. Simulation results and discussions

To verify the idea proposed in this paper, HSPICE simulation is performed in 40-inch full HDTV AMOLED panel. The simulation condition of the pixel is presented in TABLE 1.

**TABLE 1. Simulation conditions**

| | | |
|---|---|---|
| **Panel size** | | **40-inch** |
| **Resolution format** | | **Full HDTV (1920X1080)** |
| **Target luminance** | | **600 cd/m²** |
| **Required maximum current** | **Red** | **11.286 μA** |
| | **Green** | **7.050 μA** |
| | **Blue** | **12.315 μA** |
| **Data line load** | **R** | **14.08 kΩ** |
| | **C** | **250 pF** |
| **Pixel size** | | **345.9 μm X 115.3 μm** |

Fig. 5 shows the luminance error of every gray level is less than 2.6 LSB, when the maximum degradation of OLED efficiency is 30%. Fig. 6 shows the luminance errors of every gray level is less than 0.41 LSB, when the threshold voltage shift is +1V.

As we apply negative bias to the gate of driving TFT to suppress the threshold voltage shift shown in Fig. 7, we can manipulate the voltage level of the negative bias with respect to the sensed threshold voltage, which is stored in memory, so the negative bias level can be controlled less than +1V effectively.

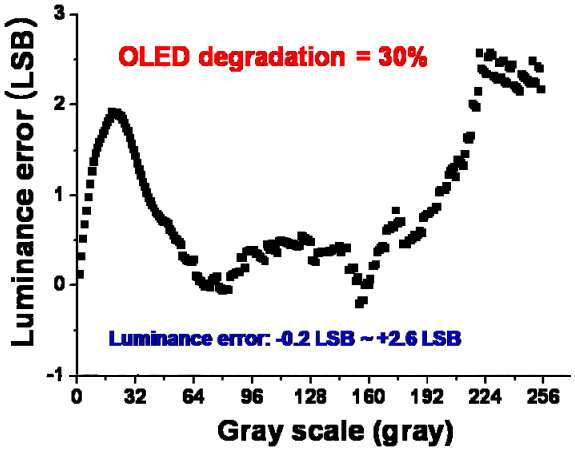


**Fig. 5. Error simulation of (a) luminance and (b) luminance error(LSB) in 30% OLED degradation.**

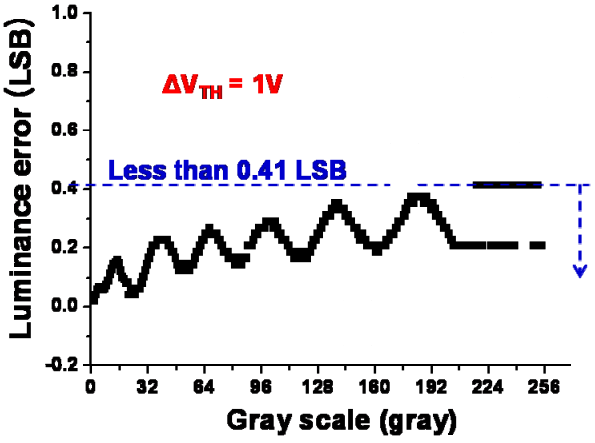


**Fig. 6. Error simulation of (a) luminance and (b) luminance error(LSB) in +1V $V_{TH}$ shift.**

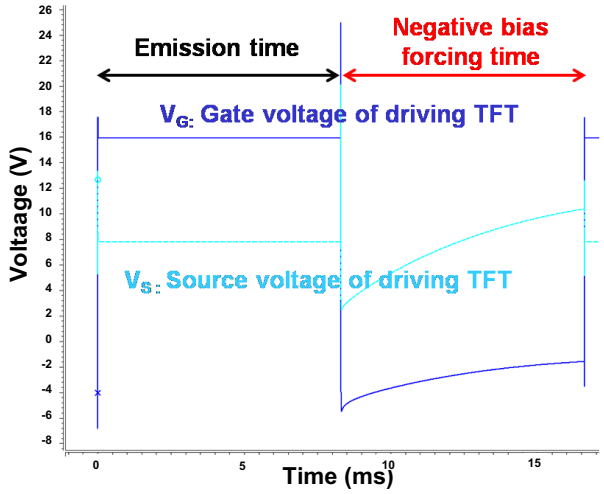


**Fig. 7. Simulation of negative bias annealing.**

## 4. Summary

This paper presents a voltage programmed driving and pixel circuits, which sense the threshold voltage of driving TFTs and the degradation of OLED efficiency, and force negative bias during dark frame insertion time. HSPICE simulation results indicate that the luminance error for every gray level is less than 0.41 LSB under the condition of +1V threshold voltage shift and 2.6 LSB under the 30% degradation of OLED in 40-inch full HDTV. As a result, we can expect that the proposed driving method can be a prominent candidate of the solution for compensation and suppression of threshold voltage shift and image sticking problems in a-Si:H TFT based AMOLED displays.

## 5. References

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