# A study on plasma-assisted patterning and doubly deposited cathode for improvement of AMOLED common electrode IR drop

***Jihoon Yang, Jeonghun Kwak, Changhee Lee, and Yongtaek Hong***
**Dept. of EECS, Seoul Nat'l Univ., Seoul, KOREA**
**Phone:+82-2-880-9567, E-mail: yongtaek@snu.ac.kr**

**Keywords : AMOLED, plasma patterning, IR drop**

## Abstract

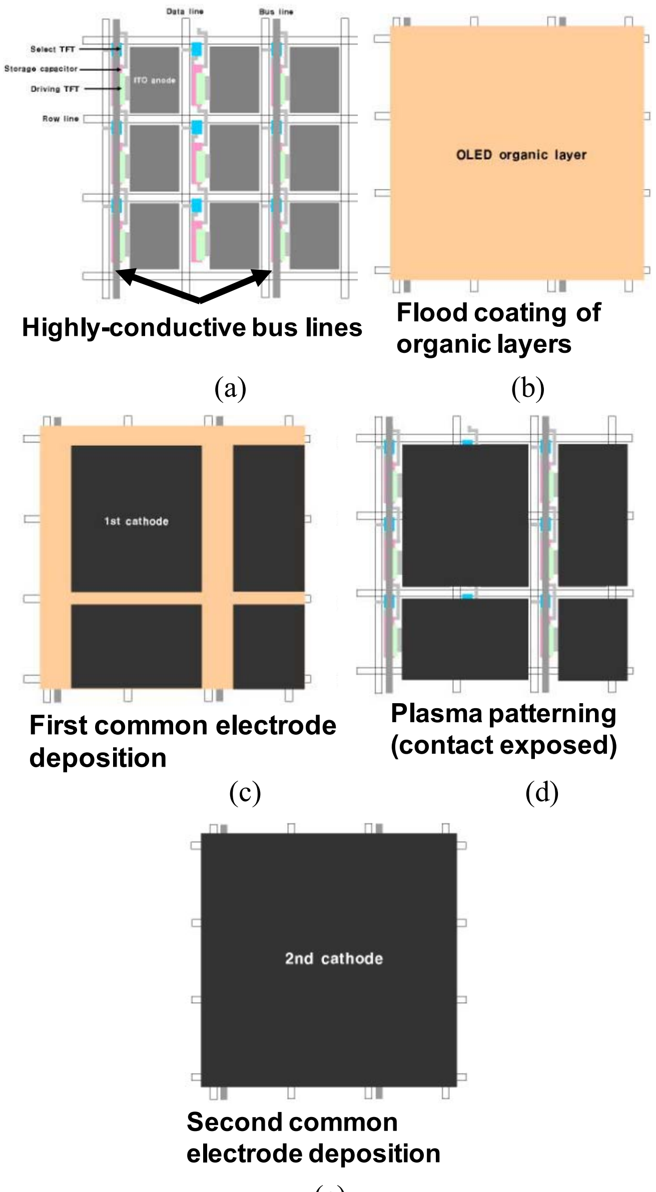
*In order to reduce IR drop through common electrode in AMOLED, we propose a novel method to form electrical contact between highly-conductive bus lines and common electrode by using a plasma-assisted patterning of OLED layers and double deposition of the common electrode. Plasma-assisted patterning effects on OLED performance and degradation have been investigated. This patterning method caused turn-on voltage decrease, current flow increase at the same applied OLED voltages, quantum efficiency decrease, and rapid degradation at early stage during the lifetime test. However, comparable 70% luminance lifetime were obtained for both patterned and non-patterned OLEDs.*

## 1. Introduction

Active-matrix organic light-emitting diode display (AMOLED) is now at mass-production stage for small to medium size display applications. In addition, many companies announced that medium to large size AMOLED television would be produced in the near future. Although organic light-emitting diode (OLED) technology has many advantages, such as, wide viewing angle, wide color gamut, high contrast ratio, low power consumption, and ultra-slim and ultra-light display implementation, there are still many technical challenges for large size display applications.

One of the key technical challenges for large size AMOLED, especially for AMOLED with top-emission pixel structures, is a large voltage drop (IR drop) along the common electrode lines due to the relatively large resistance of the semi-transparent electrode for the top-emission OLED configuration. If there is large IR drop along the common electrode lines, luminance uniformity can be significantly degraded due to different common voltages such as power supply or ground voltages, for each pixel. Therefore, additional highly-conductive bus lines are typically formed and electrically contacted to the relatively-resistive common electrode of the pixel OLEDs in order to supply current through the common line without causing any significant IR drop [1]. Highly-conductive metal grid lines have been printed on the common electrode of OLED pixels. Especially, for top-emission pixel structure, highly-conductive metal grid lines, such as silver or copper grid lines, can be printed on the common transparent electrode such as ITO electrode [2]. A laser-assisted drilling method has also been proposed to form via through the OLED layers and then expose contact area before top-electrode (common electrode) deposition. When the top-electrode is deposited, an electrical contact with the highly-conductive bus lines is formed [3]. In this case, since OLED pixel deposition process needs to be interrupted to make via and electrical contact between the common electrodes and the bus lines, interface between organic layers and the top-electrode can be degraded.

In this paper, we propose a novel method to form electrical contact between highly-conductive bus lines and the relatively-resistive common electrode by using a plasma-assisted patterning of OLED layers and double deposition of the common electrodes. Especially for AMOLEDs having white OLED with color filter array, this method would work better than other proposed methods. Plasma-assisted patterning can be easily introduced to a conventional AMOLED process. Schematic description of the proposed process for AMOLED applications is shown in Fig. 1. After bottom-electrodes of the pixel OLEDs and highly-conductive bus lines are defined (a), OLED layers can be flood-coated without any shadow masks (b). Bus lines can be added for each pixel or every 2x2, 3x3, 4x4 pixels and so on, in vertical or horizontal direction only, or in a grid format. According to the bus line design, the first shadow mask pattern for top electrodes will be determined. After the first top electrodes are deposited (c), flood-coated OLED layers will be etched by using oxygen plasma to expose the highly-conductive bus lines (d). And then, the second common top electrodes will be deposited to make an electrical contact between the first top electrodes and the bus lines (e). To investigate the feasibility of the proposed method, we analyzed the influence of oxygen plasma patterning of the organic layers on OLED device performance and lifetime.



(a) (b)

(c) (d)

(e)

**Fig. 1 Proposed plasma-assisted patterning method for AMOLEDs, especially for AMOLEDs with white OLED layers and color filter arrays)**

## 2. Experimental

Figure 2 shows fabrication process of bottom-emission OLEDs that were used in this study. Indium-tin-oxide (ITO) patterned glass substrates were cleaned in ultrasonic bath of isopropyl alcohol, acetone and methanol and then dried in a vacuum oven. The cleaned ITO surface was treated in ultraviolet (UV) ozone in 5 minutes before organic layer deposition. In this study, ITO was used as anode and bus lines for convenience (a). Thermal evaporation method was used for deposition of organic layers and cathode. All the deposition process was done at the base pressure of $2.1 \sim 8.6 \times 10^{-6}$ Torr. Organic layers consist of three materials. We used 4,4',4"-tris (3-methylpheny-phenylamino) triphenyla mine (m-MTDATA) as hole injection layer (HIL) material, 4,4'-bis [N-(1-napthyl)-N-phenyl-amino] biphenyl ($\alpha$-NPD) as hole transport layer (HTL) material, and tris-(8-hydroxyquinoline) aluminum ($Alq_3$) as electron transfer layer/light emissive layer (ETL/LEL) material. Thickness of each layer was 15, 60, and 70 nm, respectively. Green light mission (520 nm peak spectrum) was obtained from the fabricated OLEDs. The first cathode was deposited through a shadow mask. 5 nm thick lithium fluoride (LiF) and aluminum layer was deposited. Thickness of the aluminum layer was varied to find the minimum thickness required for oxygen plasma etch mask. Based on our preliminary results, the aluminum thickness should be thicker than 20 nm for the etching equipment that we used. The area of the first cathode was larger than the actual emitting area ($2\times1.4$ mm$^2$) by 0.3 mm along one direction. After fabrication, samples were transferred in air to the oxygen plasma chamber. To compare the device performances, other devices were also exposed to air for the time period equivalent to the transfer process. The samples transferred to the oxygen plasma chamber were etched in 0.1 torr and 60 sccm $O_2$ gas flow with 150 W power levels for 4 minutes (c) [4]. After oxygen plasma etching, all the samples transferred back to the OLED deposition chamber and then 100 nm thick second aluminum cathode was deposited (d). Finally all the samples were encapsulated with glass caps and UV curable glue. The whole oxygen plasma etching process including transfer processes took about 15 minutes.

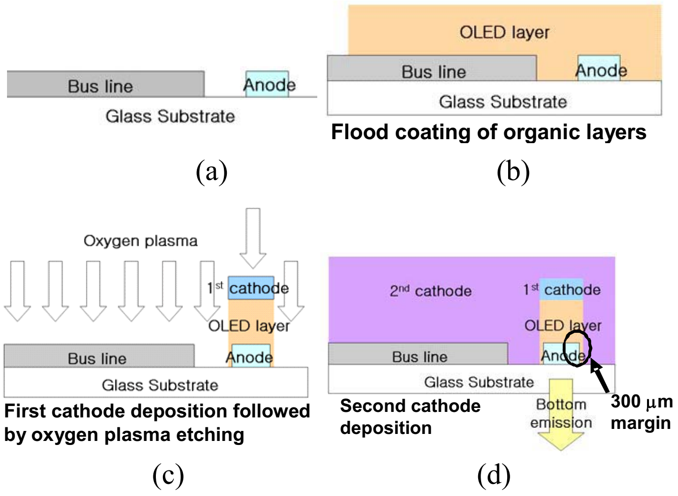


**Fig. 2 OLED fabrication process**

OLED characteristics were measured by using Keithley 236 voltage/current source, Keithley 2000 multimeter and ARC spectropro-275 monochrometer. External quantum efficiency was extracted from the measured spectral distribution and luminance data. Lifetime was measured by using Mcscience MC9600 system and changes in voltage and luminance were monitored by applying constant current. All the measurements were performed in air.

## 3. Result and discussion

Figure 3 shows current and luminance versus voltage characteristics for the fabricated fresh OLEDs. Dotted and solid lines represent the measured data for etched and non-etched OLEDs, respectively. There are some variations in current and luminance levels at the same voltage levels. We believe that these variations are related to the exposure of the devices to air during the transfer process. In fact, we observed some dark spots for OLEDs exposed to air, which can cause non-uniform device performances [5]. Although air exposure can have additionally different effects on the device performances, it is assumed that similar performance changes occurred for our fabrication processes because we tried to minimally and equally expose both devices to air during the whole fabrication process. Based on our experiment, the etched OLEDs commonly showed relatively higher current and luminance levels at the same voltages over low voltage ranges. However, as the voltage increases the current and luminance levels start to converge for etched and non-etched devices. It is believed that any defects created at the etched sides of OLED layers can cause additional current flow for low operation voltages and as voltage increases, the current flow that actually contributes to light emission increases, becoming a dominant element of the whole device current flow in comparison with the leakage current through the defects [6]. It is also commonly observed that the etched devices showed low turn-on voltages around 2V while the non-etched devices showed relatively high turn-on voltages around 3V. In this case, the turn-on voltages were defined as the voltages where the current flow increases in a step-wise manner for the semi-log current-voltage plots as shown in Fig. 3.

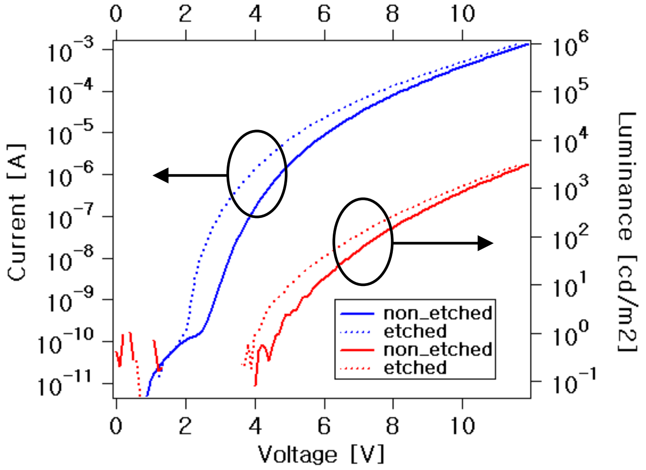


**Fig. 3 Current and luminance versus voltage characteristics of the etched and non-etched OLEDs**

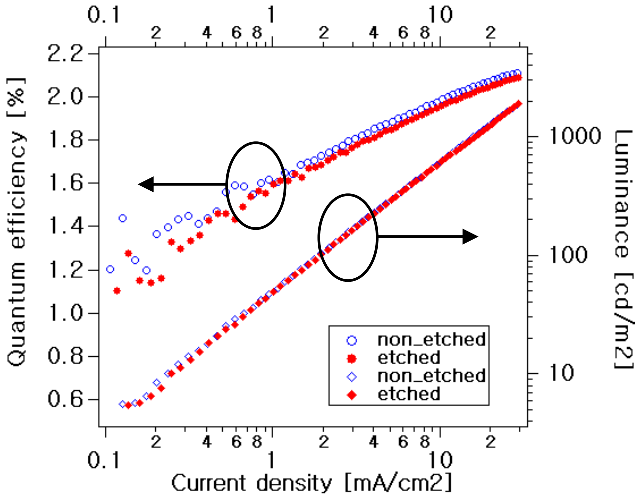


**Fig. 4 Luminance and external quantum efficiencies versus current density characteristics of the etched and non-etched OLEDs**

Figure 4 shows luminance and external quantum efficiency versus current density for the same devices used to produce Fig. 3. External quantum efficiencies of the etched OLEDs are comparable to those of the non-etched devices. We observed that performance variations within about 0.2 % from batch to batch due to the temperature and humidity variations because we had to expose devices to air during the process. However, in general, at the same current densities, luminance and external quantum efficiency were comparable for etched and non-etched devices from the same batches

We measured lifetime of both OLEDs by applying constant current to produce the same luminance of 1600 cd/m$^2$. The initial voltage and current at this luminance were 12.784 V and 0.697 mA, and 12.243 V and 0.7 mA, for etched and non-etched OLEDs, respectively. Figure 5 shows the voltage change and relative luminance progression with operation time. At early stage of the lifetime test, etched OLED rapidly degrades in comparison with the non-etched OLED. However, around 70% luminance ranges both degradation curves start to cross over and the etched OLED showed larger luminance reduction as operation time increases thereafter. When the initial luminance reaches 70% of the initial luminance, the operation time and voltage increase were 82.4 and 83.6 hours, and 0.82 and 0.899 volts for etched and non-etched OLEDs, respectively. At this stage, we do not have clear explanation for this cross-over for the lifetime test, it should be noted that the plasma-assisted etching process did not much affect the OLED performances and lifetime behaviors.

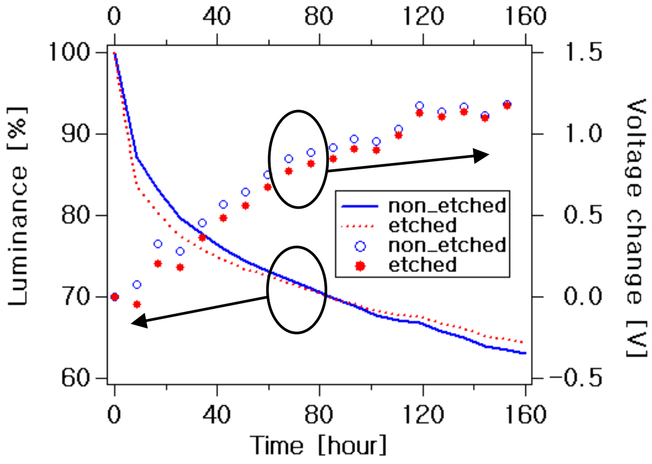


**Fig. 5 OLED luminance and voltage change with the stress time. Initial luminance was 1600cd/m$^2$ for both etched and non-etched OLEDs**

## 4. Summary

We proposed that plasma-assisted patterning method can be used to solve IR drop problem in AMOLEDs and studied its effects on OLED performances and lifetime to investigate the feasibility of the proposed method since it is believed that plasma etching process can damage organic layer and cause performance degradation. We demonstrated comparable device performances and lifetime for etched and non-etched devices. It is noted that although there is some increase in current flow for the etched OLEDs, there is only small changes in external quantum efficiencies and lifetime behavior. We believe that this method can be easily applied to the conventional AMOLED process because one additional shadow mask and oxygen plasma process are needed.

## 5. Acknowledgement

This work was supported by SSDIP (SNU-Samsung SDI Display Innovation Program). Authors would like to thank Display Technology Research Center (DTRC) and Inter-University Semiconductor Research Center (ISRC) at Seoul National University for their utility support.

## 6. References

1. G. Gu, Stefan R Forrest, *Selected Topics in Quantum Electronics*, *IEEE Journal of*, 4. 1. 83-99 (1998)
2. M. K. Kand and L. J. Guo, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 25. 6. 2637-2641 (2007).
3. Corey M. Dunsky, *Proc. SPIE*, Santa Clara, CA, USA, 5713. 200-214 (2005)
4. E. Stoffels, W. W. Stoffels, D. Vendor, M. Kando, G. M. Kroesen, and F. J. de Hoog, *Phys. Rev. E.* 51. 3. 2425-2435 (1995)
5. Masamichi Fujihira, Lee-Mi Do, Amane Koike, and Eun-Mi Han, *Appl. Phys. Lett.* 68, 1787 (1996)
6. S. Steudel, K. Myny, S. D. Vusser, J. Genoe, and P. Heremans, *Appl. Phys. Lett.* 89, 183503 (2006)