OLED Analog Behavioral Modeling Based on Physics

Sang Gun Lee, Reiji Hattori
Dept. of Electronics, Kyushu University, Motooka, Nishi-ku, Fukuoka 819-0395, Japan
TEL:81-92-802-3731, e-mail: hattori@ed.kyushu-u.ac.jp

Keywords : OLED, SPICE, Physical model, Verilog-A language, device simulation

Abstract

The physical OLED analog behavioral model for SPICE simulation has been described using Verilog-A language. The model is based on the carrier-balance between the hole and electron injected through Schottky barrier at anode and cathode. The accuracy of this model was examined by comparing with the results from device simulation.

1. Introduction

The driving method of active matrix organic light emitting display (AMOLED) is more complex than that of liquid crystal display (LCD) because it needs to be operated in an analog mode. The variation of thin-film transistor (TFT) which controls the current level through the OLED must be canceled by additional compensation circuit which is, for example, used in the voltage-programmed or current-programmed pixels. To design these complicated circuits, the precise analog circuit simulation on the pixel circuit including the OLED is necessary. Therefore, the analog behavior model for OLED device is strongly demanded.

There are two types of analog behavior models; an empirical model and a physical model. The former just represents the relation between the current and voltage, so that the parameters used in this model do not have any physical meaning. One the other hand, the later is based on the physical equations, so that all the parameters have physical meaning and the model can be applied in a wide range of temperature and device size with a simple unique equation. The physical model is also valuable for understanding the electric conduction in OLED, which has not made clear yet.

The objectives in this work to establish the physics-based OLED analog behavior model for SPICE simulation. We have described the model using the Verilog-A language that is the analogue expansion of Verilog-HDL and renowned for its logical description language.

In this study, firstly we presented the results of OLED device simulation in the simple ETL/HTL structure. All the parameters contributing to the electronic transport were extracted from the device simulation results. Next, the theoretical current density-voltage (*J-V*) characteristic equation was derived by the extracted parameters. And also the SPICE model described by Verilog-A language was created based on the theoretical *J-V* characteristic equations. Finally, we were confirmed that the *J-V* characteristics of device simulation and Verilog-A model are identical to each other.

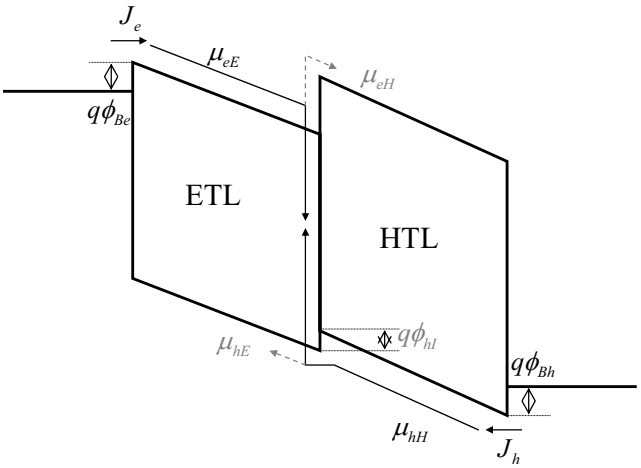

Fig. 1. Energy band diagram of two layer OLED device.

2. OLED device simulation

Figure 1 shows a typical energy band diagram for OLED composed of an electron transport layer (ETL) and hole transport layer (HTL) used in the simulation. The subscripts of e and h indicate the parameter for

electron and hole, respectively. And the subscripts of E and H indicate the parameter for ETL and HTL, respectively. The light emission occurs in ETL since the internal energy-band offset for electrons was assumed to be much higher than that for holes.

Table 1. Material parameters used for the device simulation

Parameters	ETL	HTL	Units
Barrier height	0.1~0.5	0.1~0.5	eV
Band gap	2.6	3.2	eV
Electric affinity	3.1	2.2	eV
Zero field mobility	5E-4	5E-5	$cm^2V^{-1}s^{-1}$
PF activation energy	0.48	0.48	eV
PF factor	3.7E-4	3.7E-4	
Relative permittivity	3	3	
Effective DOS	2.5E+19	2.5E+19	cm^{-3}
Thickness	50	50	nm

We have simulated the *J-V* characteristics first by changing all parameter values related to the electrical conduction using the 2-D device simulator, ATLAS (Silvaco Co.) in order to evaluate how each parameter affects the *J-V* characteristics. Table 1 shows typical parameter values used in the simulation, which were referred from the literatures. The simplified Poole-Frenkel mobility model described later was employed. For simplicity, the defect model related to the organic material was not considered in this time.

The bilayered OLED has an internal hetero-junction interface between ETL and HTL. Firstly, energy-band offset for holes (ϕ_{hI}) were varied for the simulation by changing the energy band gap of ETL. Figure 2 shows the *J-V* characteristics for different ϕ_{hI} varying from 0.1eV to 0.5eV. The internal energy-band offset for electrons (ϕ_{eI}) was fixed sufficiently high at 0.9eV to prevent the injection of electrons into HTL. We found that the change of ϕ_{hI} has no influence on the *J-V* characteristics. The reason is because more holes are accumulated in HTL near the interface with increase of ϕ_{hI} keeping the same height from quasi-Fermi level of HTL to HOMO (Highest Occupied Molecular Orbital) level of ETL, which results in the same emission rate of hole through the ϕ_{hI}. Consequently, the value of ϕ_{hI} does not need to be considered in theoretical *J-V* equation. But it is regarded to be an important parameter in terms of the device lifetime and transient characteristics.

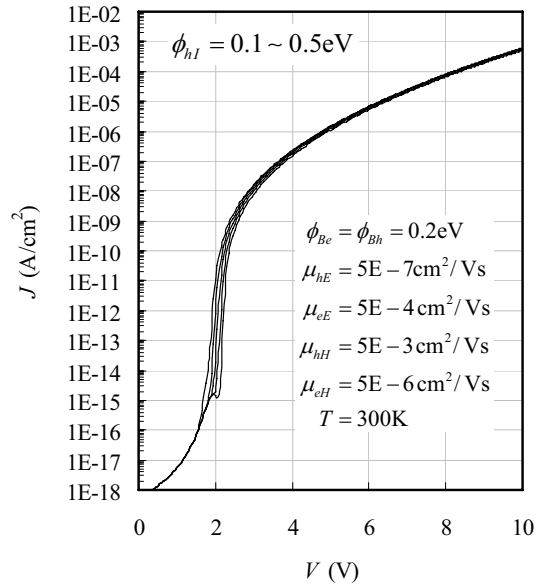

Fig. 2. *J-V* characteristics for different internal energy-band offset for holes (ϕ_{hI})

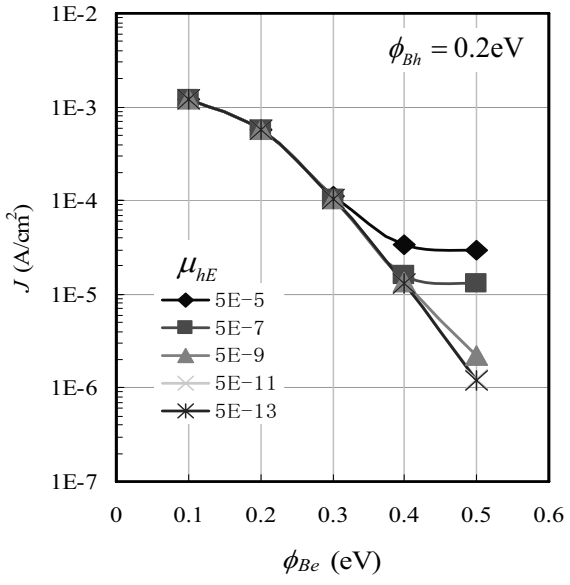

Fig. 3. *J-*ϕ_{Be} characteristics for different hole-mobility in ETL at 10 V

Figure 3 shows the current density dependence on the electron barrier height at cathode (ϕ_{Be}) for different hole-mobility (μ_{hE}) in ETL at 10V in applied voltage. We found that the current density is almost independent of μ_{hE} but influenced only in the case of ϕ_{Be} higher

than 0.4eV and μ_{hE} larger than 5E-7cm^{2}s^{-1}V^{-1}. The current density has constant value on ϕ_{Be} under these conditions. The reason is because few electrons are injected into the ETL and the electrons do not exist in the LUMO (Lowest Unoccupied Molecular Orbital) level, the holes can not recombine with electrons in ETL and the holes directly reach to a cathode under these conditions. This is the situation where the carrier balance is not kept and the OLED device behaves just like a hole-only device. However, these conditions are extremely spatial case and usual OLED does not have such conditions.

We also confirmed that the electron mobility in HTL (μ_{eH}) did not affect the *J-V* characteristics, which was obvious since the simulation was done under the conditions where no electrons are injected into the HTL.

From these results, we have revealed the important facts; (i) the electron-mobility in HTL (μ_{eH}), (ii) the hole-mobility in ETL (μ_{hE}) and (iii) the internal energy-band offset for holes (ϕ_{hI}) have no influence on the *J-V* characteristics under the ordinary conditions. Consequently, these three parameters can be eliminated in the theoretical *J-V* equations. Oppositely, all the other parameters have to be included in those equations.

3. Derivation of theoretical *J-V* equation

Next, we derived theoretical *J-V* equation from the device simulation results. These facts lead to the carrier-balance equation as follows:

$$J_e = J_h = J\,, \tag{1}$$

where J_e and J_h are the current densities for electrons and holes, respectively, and J is the total current density. In case of the low mobility, which is valid for almost all organic semiconductor materials, the carrier injection obeys a diffusion model. So we assumed that the injected carriers through Schottky barrier changes according to the equation of diffusion theory [1], which is given as follows:

$$J_e = q\mu_{eE}E_E N_{Ce}\exp\left(-\frac{q\phi_{Be}}{kT}\right), \tag{2}$$

$$J_h = q\mu_{hH}E_H N_{Vh}\exp\left(-\frac{q\phi_{Bh}}{kT}\right), \tag{3}$$

where N_{Ce} and N_{Vh} are the effective density of states (DOS) in ETL and that in HTL, respectively, and E_E and E_H are electric fields in ETL and HTL, respectively. We assumed that E_E and E_H are constant, which was found to be accurate in the case when ether of Schottky barrier heights, $q\phi_{Be}$ or $q\phi_{Bh}$, is higher then 0.2eV as shown later. In other words, the space charge effect must be taken into account under conditions where both of electron and hole barrier heights at the contacts are lower than 0.2eV. The difference between the work functions of cathode and anode metals corresponds to the built-in voltage (V_{bi}) and the flat band condition is given when V_{bi} is applied between the cathode and anode. Therefore, the relation among the applied voltage (V), E_E and E_H is given as follows:

$$V = E_E d_E + E_H d_H + V_{bi}\,, \tag{4}$$

where d_E and d_H are the thicknesses of ETL and HTL, respectively. Therefore, by combining these four equations, the relation between J and V is given as follows:

$$J = \left[\frac{d_E}{q\mu_{eE}N_{Ce}}\exp\left(\frac{q\phi_{Be}}{kT}\right)+\frac{d_H}{q\mu_{hH}N_{Vh}}\exp\left(\frac{q\phi_{Bh}}{kT}\right)\right]^{-1}(V-V_{bi}) \tag{5}$$

This equation gives the linear relationship between J and V. In case of organic materials, the mobility usually has the Poole-Frenkel type field dependence [2]:

$$\mu = \mu_0\exp\left[\frac{-\varepsilon_a}{kT}+\frac{\beta\sqrt{|E|}}{kT}\right], \tag{6}$$

where μ_0 is the zero field mobility, and ε_a the thermal activation energy of organic material at zero electric field, β Poole-Frenkel factor. The barrier height also has filed dependence as barrier lowering:

$$\phi_B = \phi_{B0} - \frac{\alpha\sqrt{|E|}}{kT}, \tag{7}$$

where E is the magnitude of the electric field at the interface and α is linear constant. The model incorporates the image force barrier lowering at contacts.

As a result, Eq. (5) gives the exponential increase with the applied voltage, but the equation including the field dependence of mobility and the barrier height are too complicated to be simplified algebraically as a function of V, anymore.

In order to solve Eqs. (1)~(7) simultaneously, we employed the equivalent circuit shown in Fig. 4. The built-in voltage (V_{bi}) is expressed by the voltage source. Once the equation representing the relationship between output and input are obtained, it is easy to generate the analog behavior model using Verilog-A language. In addition, since the Verilog-A language can treat an internal node, it is possible to solve the simultaneous equations even if the equations are not solved in an algebraic manner. The *J-V* characteristics from the model described with Verilog-A language are shown in Fig. 5. Assuming a constant field in each layer, the fields, E_E and E_H, are given by dividing the voltages applied on each diode by each layer thickness. Eq. (1) is automatically satisfied by connecting the diodes in series.

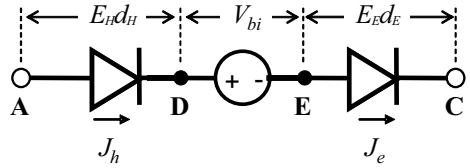

Fig. 4. Equivalent circuit in Verilog-A model

4. Comparison between the device simulation and Verilog-A model

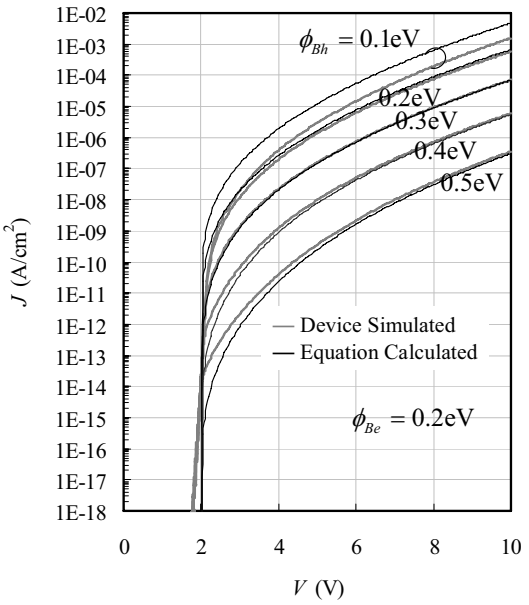

Fig. 5. Comparison between the device simulation and Verilog-A model

Figure 5 shows the comparison of *J-V* characteristics between the results from device simulation and SPICE circuit simulation using the Verilog-A as a parameter of Schottky barrier height for hole at anode. The barrier height for electron at cathode (ϕ_{Be}) was fixed at 0.2eV. In both calculations the same physical model and parameters were employed. As shown in Fig. 5, a relatively good agreement between both results was obtained expect for the cases of low voltage range and the case of ϕ_{Bh}=0.1eV. The reason for deviation in low voltage range is that no calculation of reversely diffused current in Verilog-A model is considered. The deviation in the results at ϕ_{Bh}=0.1eV is due to a space charge effect. This fact means that the space charge effect does not occur until the barrier height gets so low. However, this effect is significant in the case of good contact OLED. Therefore, we are planning to include this effect in the model of Verilog-A.

5. Conclusions

We successfully derived theoretical *J-V* equations form the device simulation results. These theoretical equations include all the parameters related to the electric transport but exclude the parameters of the electron-mobility in HTL, the hole-mobility in ETL and the internal energy-band offset for holes because they have no influence on *J-V* characteristics. Using these equations, we described a SPICE model using Verilog-A language showing a good agreement with the results calculated from the device simulation.

6. Reference

1. S. M. Sez, physics of semiconductor Device, *Wiley New York,* **2nd edition**, pp 254-270 (1981).
2. J. L. Egley, and D. Chidambarrao, *Solid-State Electronics*, **36**, pp 1653-1664 (1993).