Effects of Address Electrode Width on Address Discharge Under Variable Ambient Temperature in AC-PDP

Soo-Kwan Jang[1], Heung-Sik Tae[1], Eun-Young Jung[2], Jung-Chull Ahn[2] and Minsun Yoo[2]
[1]School of Electrical Engineering and Computer Science Kyungpook National University, Daegu 702-701, Korea
TEL:82-53-950-6563, e-mail: hstae@ee.knu.ac.kr.
[2]R&D Team, PDP Division, Samsung SDI co. Ltd, Chungchongnam-Do 330-300, Korea

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Abstract

It is known that the address discharge delay time during an address period strongly depends on the wall charge leakage. It was observed that the wall charge leakage during an address period is related to both the address width and the ambient temperature. Accordingly, the effects of address electrode width on the address discharge and wall voltage variation during an address period were examined under variable temperatures.

1. Introduction

Although the image quality of plasma display panels has continued to improve significantly, further advances in the image quality of ac-plasma display panels, especially full high definition (HD) PDPs, require a wider driving margin and more stable discharge. The ambient temperature is one of the important factors for producing the stable discharge in the PDP cells because the discharge characteristics are varied depending on the ambient temperature [1]. The misfiring discharge at a high temperature was often observed, especially address discharge failed at the upper sub-field. This is deeply related to the wall charge leakage phenomenon during an address period. The wall charge leakage was increased with an increase in the number of applied address and sustain pulses, and this tendency was intensified with an increase in the ambient temperature [2].

In this paper, the effects of address electrode width on the address discharge and wall voltage variation during an address period were examined under variable ambient temperature.

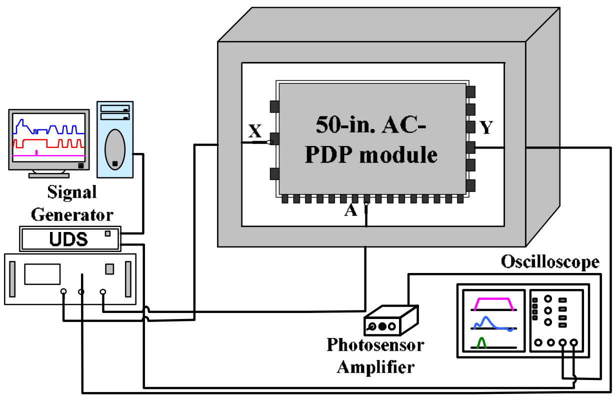

Fig. 1. Schematic diagram of experimental setup for overall heating of 50-in. test panel

TABLE 1. Specifications of 50-in. test panel employed in experiments.

Specifications of 50-in. test panel	
Pixel pitch	808 μm
Rib Height	120 μm
Gas mixture	Ne - He (35 %) - Xe (11 %),
Pressure	450 Torr
ITO width	310 μm
ITO gap	60 μm
Address electrode width	**Case I** : 60 μm **Case II** : 90 μm **Case III** : 120 μm **Case IV** : 150 μm

2. Observation of discharge characteristics related to the address electrode width

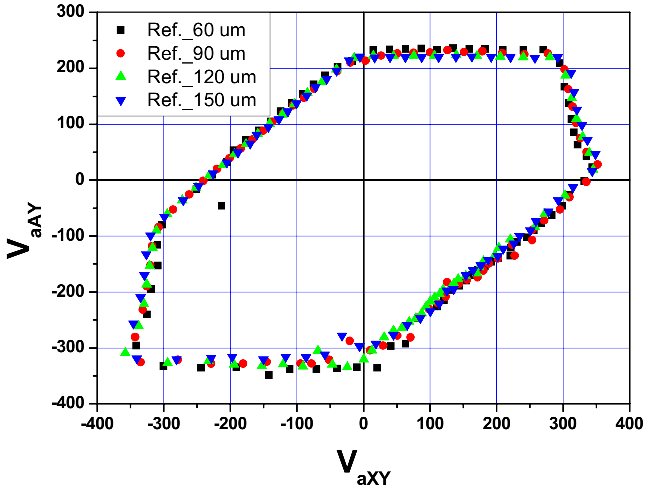

Fig. 2. Vt closed-curves measured from 50-in. panel relative to address electrode width from 60 μm to 150μm.

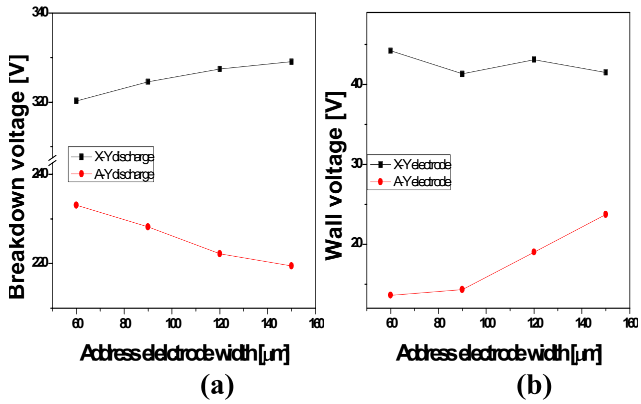

Fig. 3. Variation of (a) firing voltage and (b) wall voltage of A-Y and X-Y electrode formed through reset discharge relative to address electrode width.

Fig. 1 shows the schematic diagram of the experiment setup for measurement. The ambient temperature of the test panel was varied from -5 to +65 ^{O}C by heating of cooling the temperature test-chamber. To avoid the influence of the ambient temperature on the electronic circuit, all the electronics were positioned outside the temperature test-chamber. The 50-in. panel with a working gas pressure of 450 Torr was employed in the research, and its structure and dimensions were the same as the conventional 50-in. wide XGA grade PDP with a box-type barrier rib. The used gas mixtures were He-Ne-Xe (11%). When the address electrode width was varied from case I to case IV, the wall charge leakage

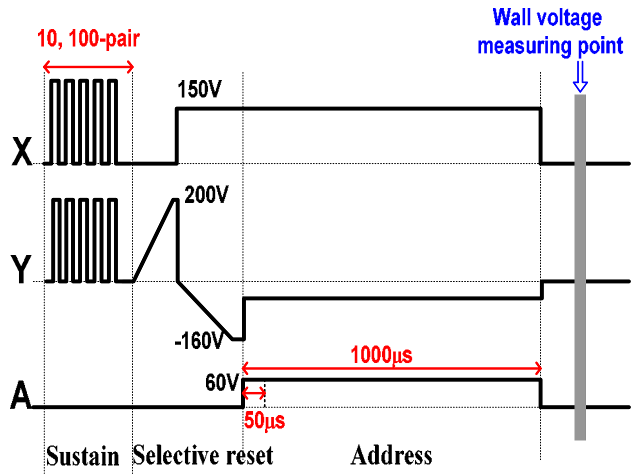

Fig. 4. Driving waveform employed in experiments to measure wall charge leakage during address period and related address discharge.

during an address period and related address discharge characteristics were investigated.

Fig. 2 shows the Vt closed-curves relative to the address electrode width under zero initial wall voltage conditions. When the address electrode width was increased from 60 to 150 μm, the plate gap discharge between the A-Y electrodes has more influenced than the surface discharge between the X-Y electrodes. As shown Fig. 3 (a), the firing voltage of the A-Y discharge was increased (Δ V = +14 V) relative to the address electrode width from 60 to 150 μm, whereas the firing voltage of the X-Y discharge was decreased (Δ V = -8 V). This phenomenon was mainly due to the change in the capacitances among the three electrodes. That is, the capacitance between the A-Y electrodes was increased relative to the address electrode width from 60 to 150 μm, but the capacitance between the X-Y electrodes was decreased [3, 4]. Fig. 3(b) shows the wall voltage between the A-Y electrodes and the X-Y electrodes formed through the main reset discharge relative to the address electrode width. As address electrode increased from 60 to 150 μm, wall voltage between the A-Y electrodes was increased.

3. Effect of address electrode width on wall voltage variation during address period

Fig. 4 shows the driving waveform employed in experiments to measure the wall charge leakage during an address period and related address discharge

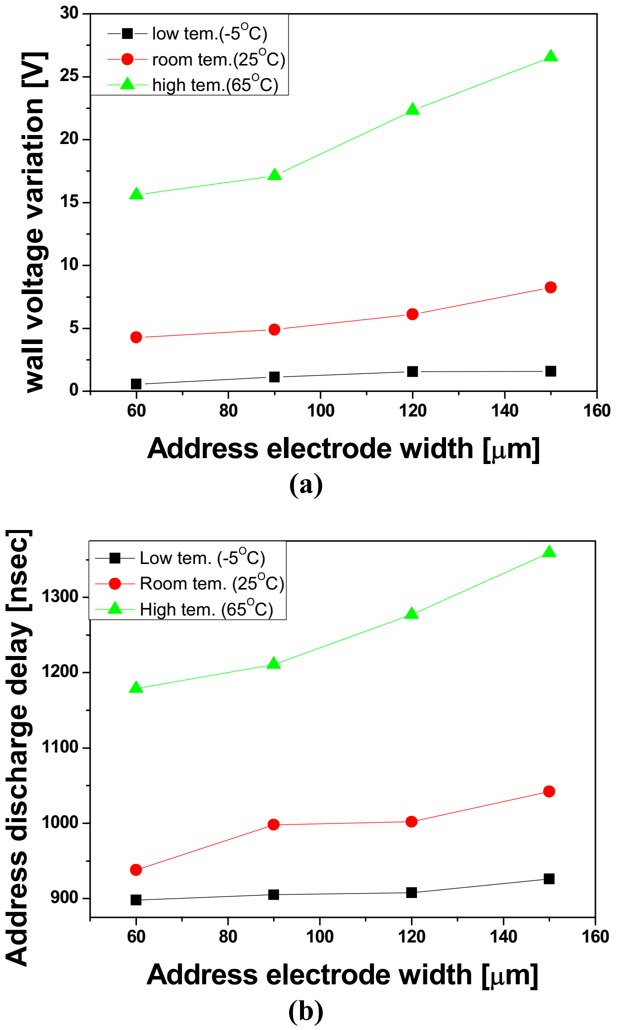

Fig. 5. Wall voltage variation during address period and address discharge delay time relative to address electrode width and ambient temperature measured at upper subfield.

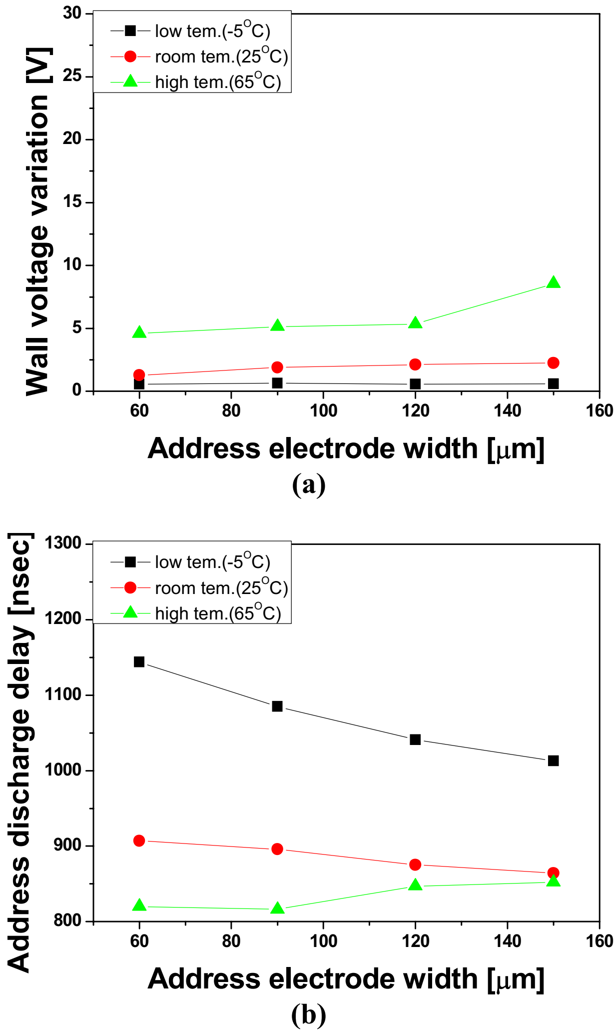

Fig. 6. Wall voltage variation during address period and address discharge delay time relative to address electrode width and ambient temperature measured at lower subfield.

relative to the applied address and sustain pulse under variable ambient temperature. The applied sustain pulses were 10-pairs for the lower sub-field (SF 3) and 100-pairs for the upper sub-field (SF 10). In addition, the conditions for address pulses are given as follows: an address pulse width of 1.25 μs, that is, the address periods were 50 μs for 40 scan lines and 1000μs for 800 scan lines. Fig. 5 (a) shows the wall voltage variation between the A-Y electrodes during address period relative to the address electrode width and ambient temperature at upper subfield. The wall voltage variation during an address period was increased relative to the address electrode width. This tendency was increased at the higher ambient temperature (-5 ^{O}C), whereas it was decreased at the lower ambient temperature (+65 ^{O}C).

Fig. 5 (b) shows the address discharge delay time relative to the address electrode width under various ambient temperatures at the upper subfield. The address discharge delay was increased according to the address electrode width at the room (+25 ^{O}C) and higher ambient temperature (+65 ^{O}C), whereas it was little changed at the lower ambient temperature (-5 ^{O}C). It is would be caused by the wall charge leakage during an address period. Fig. 6 (a) shows the wall voltage variation between the A-Y electrodes during an address period relative to the address electrode width and ambient temperature at the lower subfield. The wall voltage variation during an address period was almost the same relative to the address electrode width. As shown Fig. 6 (b), the address discharge delay time relative to the address electrode width was slightly changed at the room (+25 ^{O}C) and higher ambient temperature (+65 ^{O}C). However, at the lower ambient temperature (-5 ^{O}C), the address discharge delay time was decreased according to the address electrode width from 60 to 150 μm.

4. Summary

It is important to maintain the discharge stability, especially address discharge stability under the variable ambient temperature conditions. In this sense, this paper can contribute to producing the stable address discharge by examining the relation between the ambient temperature and the cell parameter such as an address electrode.

5. References

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