Air stable n-type organic field effect transistors using a perfluoropolymer insulator

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Abstract

Air stable n-type organic field effect transistors (OFETs) based on C_{60} are realized using a perfluoropolymer as the gate dielectric layer. The devices showed the field-effect mobility of 0.05 cm^2/V s in ambient air. Replacing the gate dielectric material by SiO_2 resulted in no transistor action in ambient air. Perfluorinated gate dielectric layer reduces interface traps significantly for the n-type semiconductor even in ambient air

1. Introduction

There has been much progress in performance of organic field effect transistors (OFETs) in recent years. A large number of semiconducting organic and polymeric materials have been reported and high field effect mobilities with high on/off ratios have been realized. Most of the materials are, however, p-type and fewer n-type materials have been reported up to now. Moreover most of the reported n-type organic semiconducting materials showed instability and sensitivity to air exposure in operation. Because accepter-like trap states caused by oxygen induce threshold voltage shift[1] and destroy OFETs performance, *in situ* measurement in high vacuum chamber or device passivation techniques are employed to characterize n-type OFETs.[2] Two methods have been reported to overcome the problem. The first one is to use specially designed semiconductor materials with strong electron withdrawing groups.[3 4 5 6] It helps to increase electron affinity and prevent reaction with moisture or oxygen in ambient air. Another one is to use large grain and highly packed polycrystalline semiconductor. It reduces penetration of moisture and oxygen into the active region of film.[7 8]

In this letter, we report another method to fabricate air stable n-type OFETs, i.e., use of a perfluorinated polymer as the gate dielectric layer. C_{60} was employed as an n-type semiconductor, which is reported to be unstable upon exposure to ambient air if the device is fabricated on SiO_2 dielectric layer.[9 10] We focused on the interface between semiconductor and insulator rather than semiconductor bulk itself. Moisture or hydroxyl group at the interface has electron withdrawing characteristics and acts as trap sites in operation of n-type OFETs. Recently, hydroxyl-free gate dielectric such as divinyltetramethylsiloxane-bis(benzocyclobutene) derivative(BCB) is reported to be able to yield n-channel FET conduction in most conjugated polymers[11]. But it is limited to passivated devices, we selected CYTOP™ fluoropolymer as dielectric insulator[12] to decrease the effect of interface trap sites and fabricated ambient air-stable C_{60} OFETs

2. Experimental

OFET devices have top-contact and bottom-gate structures. The devices were fabricated on a heavily doped silicon wafer which works as the common gate electrode. Either thermally grown SiO_2 (3000 Å) or spin-coated CYTOP™ (3600 Å) was used as the dielectric layer. Silicon dioxide substrate was cleaned with H_2SO_4:H_2O_2=4:1 solution and rinsed with dionized water. The surface was treated with UV-O_3 for 10 min before the deposition of an organic semiconductor. CYTOP™ was purchased from Asahi Glass and spin-coated on a Si wafer. Native oxide of the Si wafer was removed using buffered oxide etchant before spin coating. 50 nm thick C_{60} film was deposited onto the dielectric layers with thermal evaporation under a pressure of 2.0×10^{-6} torr. Deposition rate was 0.5 Å/s. Substrate temperature was maintained at 50 ℃ and active region was

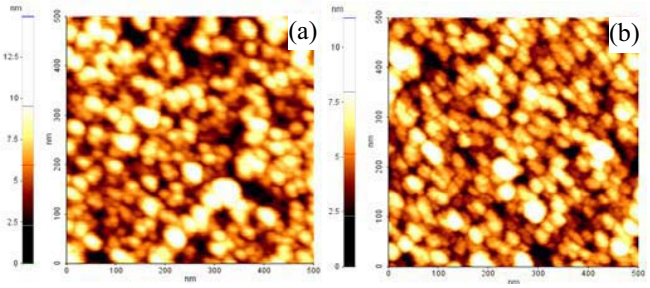

Fig. 1. AFM morphology of C_{60} on (a) SiO2 (b) CYTOP™ (Scan size is 500 nm× 500 nm)

patterned with a metal shadow mask. Au source and drain electrode were deposited by thermal evaporation under a pressure of $5.0x10^{-7}$ torr with the deposition rate of 2.0 Å/s. Channel length and width was defined to 50 μm and 500 μm, respectively, with a metal shadow mask. Thickness of the electrodes was 1000 Å. Some fabricated devices were encapsulated with glass cans in a globe box with CaO desiccant in an inert environment. O_2 and H_2O level in the globe box are under 1.0 ppm, respectively.

Electrical measurements were performed using an Agilent 4155C semiconductor parameter analyzer and a Suss PM8 probe station. All electrical measurements were made in the dark. Atomic Force Microscope (AFM) topographic images were taken in a PSIA XE-100 scanning probe microscope with non-contact mode.

3. Results and discussion

Figure 1 shows AFM images of the C_{60} films on the insulators. The root-mean-square (RMS) roughnesses of the 50-nm-thinkness C_{60} films are almost the same with 1.84 nm on CYTOP™ and 1.44 nm on SiO_2, respectively. Average grain size of C_{60} film on SiO_2 is 24.1 nm and on OTS is 25.2 nm. These films are consisted with small crystals and porous, it hard to prevent permeation of oxygen or moisture through the grain boundaries, one of the method to show stable FET characteristics in ambient air.

Drain current-drain voltage (I_D-V_D) characteristics of C_{60} based FETs with the CYTOP™ and SiO_2 insulator are displayed in figure 2 for different gate biases (V_g). The device with the SiO_2 insulator exhibits n-type characteristics only when it was encapsulated (figure 2a). The device without encapsulation does not show any transistor characteristics under exposure to air (not shown), which is consistent with the previous reports[910]. It is worthwhile to note, however, that the device with the CYTOP™ insulator shows clear n-type I_D-V_D characteristics even in air without passivation (figure 2b). If the device is

encapsulated the current was increased considerably (figure 2c).

The transfer characteristics of the devices measured just after the fabrication of the devices (t=0) in the saturation regime (V_D= 100 V) are shown in Figure 3. In the figure, the transfer characteristics of the reverse scan are shown as the dashed lines. The device with SiO_2 gate dielectric layer (figure 3a) shows the electron mobility of 0.08 $cm^2/V{\cdot}sec$, threshold voltage of 22.5 V , on-off ratio of 10^4. Moreover, the devices showed large hysteresis of 42 V.

In contrast to the device with SiO_2 insulator, the device with CYTOP™ insulator without encapsulation showed the electron mobility of 0.049 $cm^2/V{\cdot}sec$ in ambient air, which is comparable to the encapsulated device with SiO_2 gate insulator (figure 3b). It is interesting to note that the device has very large threshold voltage of 64.0 V but with very small hysteresis. The encapsulated device with CYTOP gate insulator (Figure 3c) resulted in the best device performance as expected. The device showed the electron mobility of 0.20 $cm^2/V{\cdot}sec$, threshold voltage of 29.0 V, and on-off ratio of 10^5, respectively.

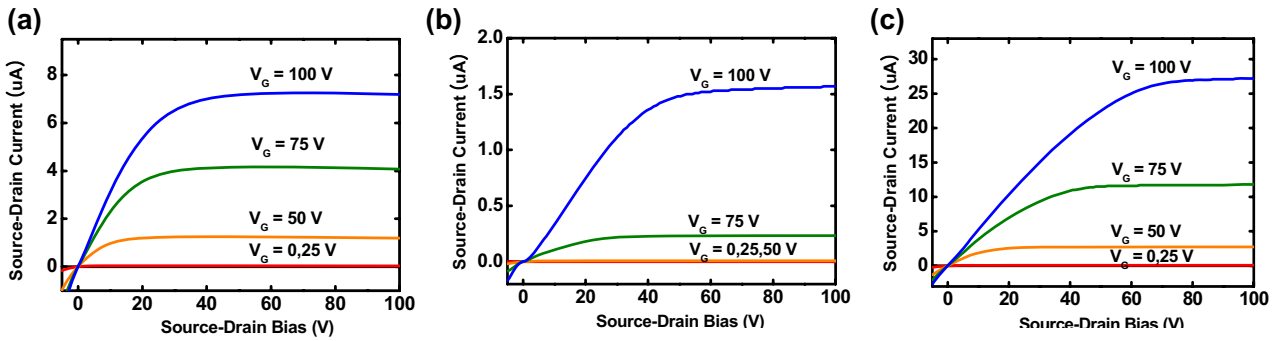

Fig. 2. output(I_D-V_D) characteristics of C_{60} OFETs with (a) SiO_2 insulator in inert environment (passivated), (b) CYTOP ™ insulator in ambient air and (c) CYTOP™ insulator in inert environment (passivated)

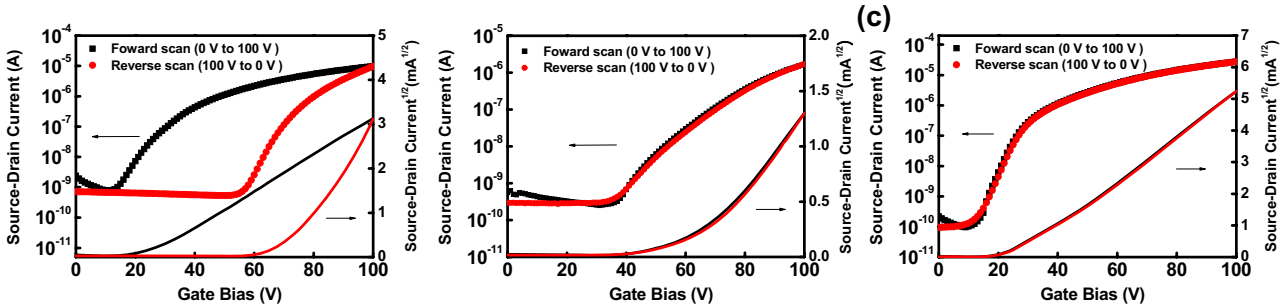

Fig. 3. transfer(I_D-V_G) characteristics of C_{60} OFETs in saturation regime (V_D = 100 V) with (a) SiO_2 insulator in inert environment (passivated), (b) CYTOP ™ insulator in ambient air and (c) CYTOP™ insulator in inert environment (passivated)

To further evaluate the stability of devices, we investigated the evolution of the transfer curves of the devices and the variation of mobility, threshold voltage and hysteresis with time are plotted in figure 4. Hysteresis in the figure was defined as the difference of gate bias between the forward and reverse scan at the source-drain current of 10 nA ($V_{hystesis}$=$V_g^{forward}$-$V_g^{reverse}$ at 10 nA).

The passivated device with SiO_2 insulator shows very large hysteresis of 42 V in the first scan. After the first scan, large threshold voltage shift more than 40 V was observed and hysteresis was reduced significantly to less than 5V. Mobility was increased to 0.12 $cm^2/V{\cdot}sec$ near the 100 sec after the initial scan but slightly decreased after that point. This phenomenon can be understood by trap states at the interface between C_{60} and silicon dioxide or thin transporting layer near the interface. As the gate bias increases in the first scan, the trap states are filled with electrons. These trapped electrons induce the hysteresis in the first scan and large threshold voltage shift from the second scan. After the originally empty deep traps are filled, charges are trapped only in shallow states. As results, the threshold characteristics do not change much and the mobility is increased.

The device with CYTOP™ insulator in ambient air shows similar characteristics as the passivated device with SiO_2 insulator after the first scan. The device shows slowly decreasing mobility with time. The threshold voltage shift and hysteresis are maintained below 5 V until 20000 sec. Almost similar threshold voltage of the unpassivated device with CYTOP™ insulator and the passivated device with SiO_2 indicates that the trap density at the interface is almost the same between the two devices and the traps are filled by the exposure to the air in the CYTOP™ devices and by the first scan in the SiO_2 device. The source of decreasing mobility is understood to continuous generation of deep trap sites near interface of semiconductor and insulator due to contact to ambient air including moisture and oxygen.

Passivated device with the CYTOP™ insulator shows most stable characteristics without any significant change up to 2000 sec after initial scanning. It had very low hysteresis (< 2 V) and low threshold voltage shift (< 2 V) up to that time. Higher electron mobility and lower threshold voltage of the encapsulated device than un-encapsulated device indicates that the traps at the interface or thin transporting layer near the interface are generated by the exposure of the device to ambient air.

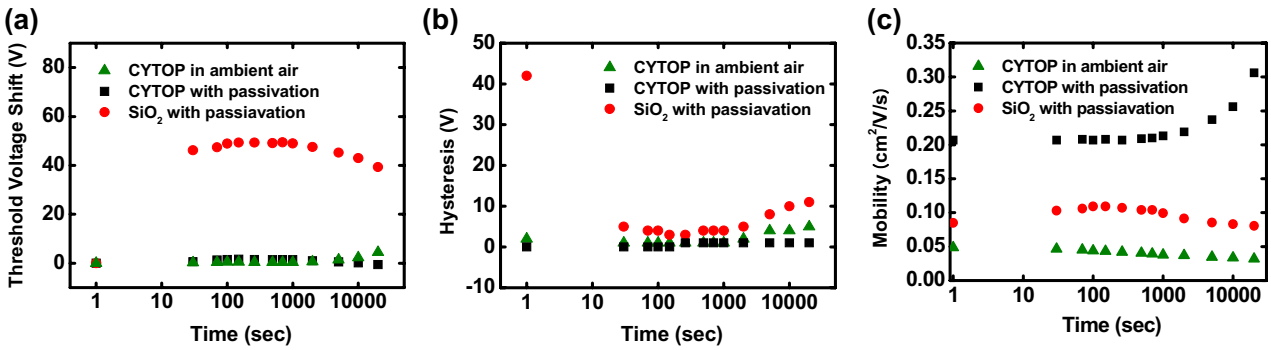

Fig. 4. Time dependence of (a) mobility (b) hysteresis (c) threshold voltage shift

4. Summary

We demonstrated an air stable n-type C_{60} OFET by using an perfluorinated polymer, CYTOP™, as the gate dielectric layer. Replacing the gate dielectric material to SiO_2 resulted in no transistor action in ambient air. The device showed similar device characteristics as the encapsulated device fabricated on SiO_2 gate dielectric layer. This indicates that the interface trap density for electrons for n-type organic materials is significantly reduced by using the perfluorinated polymer as the gate dielectric layer even in ambient air.

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5. References

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