Effect of deposition method of source/drain electrode on a top gate ZnO TFT Performance

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Abstract
We have investigated the effect of source/drain electrode deposition method on a performance of top gate structured ZnO TFT performance. TFT using S/D of ITO film, consisted of bi-layer which deposited by ion beam assisted sputtering at the initial stage then deposited by DC magnetron sputtering, showed better performance compared to that using S/D of ITO deposited by just DC magnetron sputtering. Two ITO films exhibited different grain shapes and these resulted in different etching properties. We also suspect that charge trapping on the glass substrate (back channel) during the ITO film deposition may influence the characteristics of top gate structured ZnO TFT.

1. Introduction
Oxide TFTs have been attracted lots of interests during last a couple of years due to moderate mobility, stability, and uniformity on a relatively large size substrate.[1-4] The needs for these oxide TFT have been mostly focused on the back plane of AM-Display including LCD, OLED, flexible display, and transparent display, and electronics.[5] Recently there have been many reports on the performance of oxide TFTs and AM-Display driven by oxide TFT.[6-8] Though oxide semiconductor and gate insulator processes, device structure, and post annealing process change device performance dramatically, there is another important factor to affect device characteristics in a top gate structure oxide TFT. It is a substrate surface which provides interface of back channel with active layer between source and drain electrode (S/D). Back channel could play a very important role in a TFT with thin active layer. In a TFT using ITO as S/D electrode, ITO deposition method resulted in not only different film properties but etching property to give different back channel.

We report the effect of ITO deposition method on a top gate ZnO TFT characteristic.

2. Experimental
Non alkaline glass was used as a substrate. ITO films used for S/D electrode were deposited in two ways. Film A (named as D) was deposited by DC magnetron sputtering in a 150 nm thickness and film B (named as ID) was deposited by ion beam assisted sputtering at a first stage in a 15 nm thickness then deposited DC sputtering used for the film A deposition in a 135 nm thickness to make total film thickness same.

For the fabrication of TFT, after patterning of S/D electrode by wet process, ZnO semiconductor films were deposited by means of PEALD at the RF power of 130W at 200 °C and ZnO protection layer (PL) was deposited by ALD.[9] After patterning ZnO and PL using diluted acid at once, alumina was deposited at the temperature of 150°C by means of ALD, followed by S/D electrode pad opening by wet etching of alumina. Sputtered Al film was used as a gate electrode. The structure of TFT is shown in the figure 1.

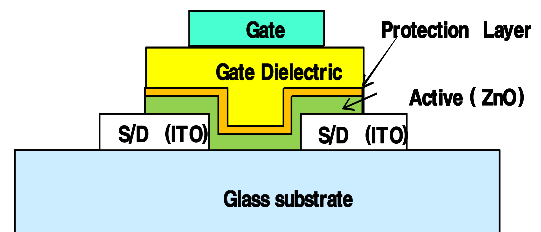

Figure 1. Schematic cross sectional diagram of ZnO TFT

3. Results and Discussion

Figure 2 shows the SEM image of grain shapes of film ID and D. While Film ID showed relatively small sized grain, film D showed big sized grain which were reported in a typical ITO film deposited at high temperature.

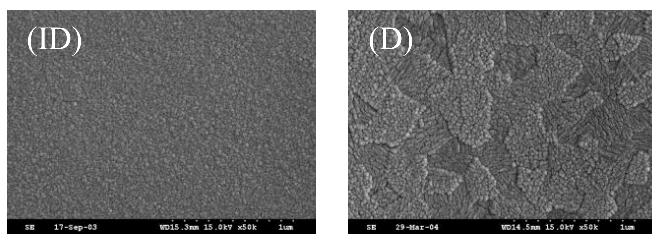

Figure 2. SEM images of Film ID and Film D (ID : ion beam assisted sputtering + DC sputtering, D : DC sputtering only)

XRD data shown in figure 3 also revealed different film properties i.e. Film ID and D have preferred orientation at (222) and (400), respectively.

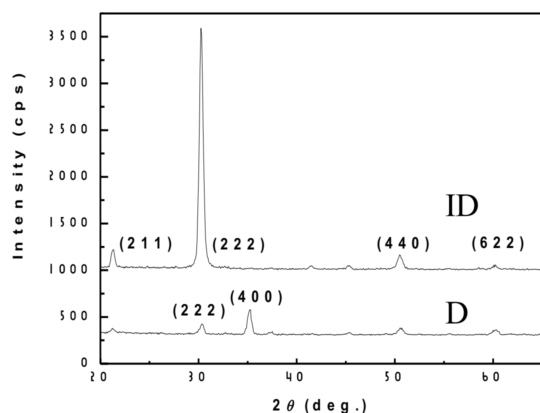

Figure 3. XRD data of Film ID and Film D (ID : ion beam assisted sputtering + DC sputtering, D : DC sputtering only)

Etching property of S/D electrode is very important in a top gate structure of TFT, for surface exposed after S/D etching forms interface of back channel with active layer. When we etched ITO films with commercially available polycrystalline ITO etchant at 40°C during same time, each substrate has different ITO residue as shown in the figure 4. While Film D left severe residue on the bare glass, Film ID has less amount of residue. Even after finishing each ITO film etching during different time, there was still residue of ITO film D on the glass surface a little. The residue was confirmed as ITO by ESCA analysis as shown in figure 5. This means that glass substrate coated by ITO grown by DC sputtering may form different back channel with that coated by ID film. This may cause different device characteristic.

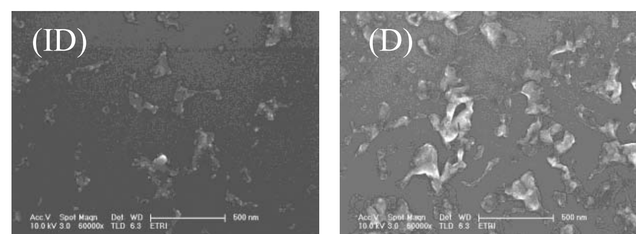

Figure 4. SEM images of ITO (Film ID and D) glass surface after ITO etching during same time

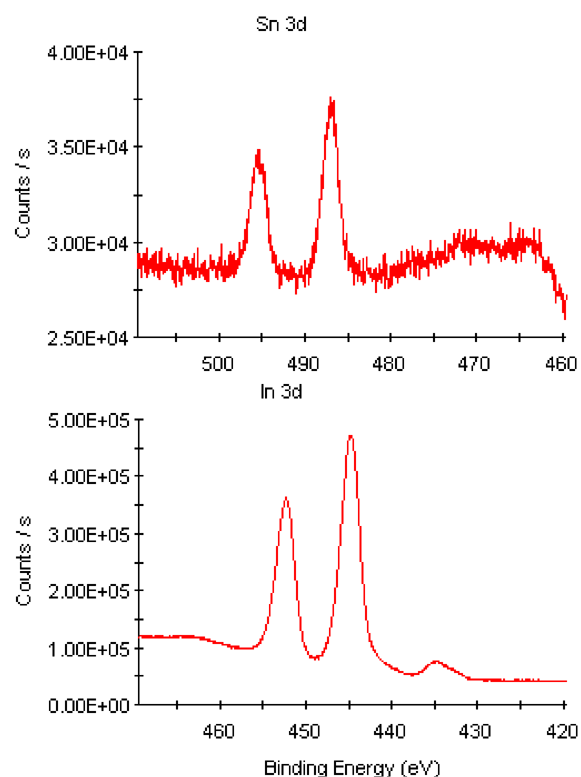

Figure 5. ESCA data of residue on the glass after finishing Film D etching

We fabricated ZnO TFTs using these two substrates with the structure shown in figure 1 by the previously reported method.[9] Figure 5 displays

performance of ZnO TFTs adopting Film ID and Film D as S/D electrode. Device with Film D shows more negative Von of -4.5 V, higher swing of 0.45 V/dec., and lower mobility of 3.36 cm^2/V.s. compared to that of device with Film ID having Von of -0.91 V, swing of 0.32 V/dec., and mobility of 3.98 cm^2/V.s.

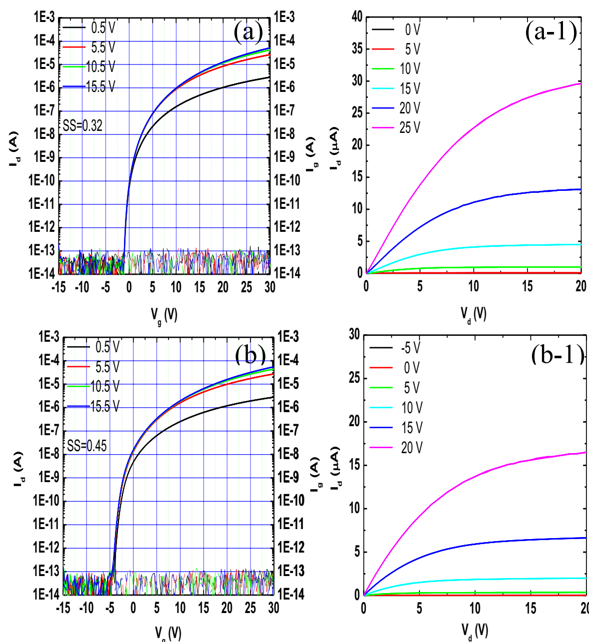

Figure 5. Transfer characteristics of ZnO-TFT with Film ID (a) and Film D (b) in W/L=40/20 for V_{DS} varying from 0.5 to 15.5V and (b) Output characteristics for a ZnO-TFT with Film ID (a-1) and Film D (b-1) in W/L=40μm/20μm.

There might be several reasons for the different TFT performance. ALD method used for ZnO active layer can provide very conformable film. Therefore, different substrate could provide different ZnO surface and this affects device characteristics due to the formation of different interface. In addition, rough back channel may affect swing and Von. However, according to our previous result[10], the substrate roughness is not the main reason for the Von negative shift. We cannot rule out the possibility of severe charge trapping in the back channel in the device with Film D since plasma damage mostly induces charge trapping. When we patterned ITO by the lift-off process, completely avoiding the plasma damage and ITO residue in the back channel, and fabricated TFT with this ITO as S/D, we could confirm the TFT characteristics with more positively shifted value.[11]

The S/D process affects even bottom gate structured oxide TFT performance. Direct dry etching of Mo S/D degraded a-IGZO TFT characteristic a lot.[4] This implies that plasma less process for the formation of back channel would improve the TFT performance.

There are several important issues on the uniformity of oxide TFT. The active layer thickness,[12] uniform composition of active layer, and well defined dimension of S/D would affect the uniformity of oxide TFT array. According to our result, in the case of top gate oxide TFT using ITO as S/D, it would be very important to form uniform back channel by clean substrate surface and plasma less process of S/D.

To implement transparent display, it is essential to use TCO such as ITO as S/D, and it is well known that complete ITO etching, even in the case of amorphous ITO, is very hard. Therefore, it is necessary to form S/D film which can reduce the plasma damage during the deposition and develop etching process of ITO film to get high uniformity of transparent backplane.

4. Summary

We have investigated the effect of S/D electrode deposition method on the top gate structured ZnO TFT performance. Device with ITO deposited by ion beam assisted sputtering at an initial stage showed better performance than that with ITO film deposited by DC sputtering. This result showed that S/D electrode deposition method is very important parameter in top gate structure since it affects the back channel. Back channel formation method would also affect even in a bottom gate structure of oxide TFT since most of oxide TFT has relatively thin active layer and following process of active layer such as S/D etching would significantly affect the device performance.

5. Acknowledgements

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