Stability of Low Temperature a-Si:H TFT on Stainless Steel Substrate

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Keywords : TFT, Stainless Steel, Flexible, Low Temperature, Stability

Abstract

Low Temperature a-Si:H TFT on stainless steel substrate has been developed for the flexible electrophoretic display. Stability of low temperature a-Si:H TFT is more important point than its initial device characteristics. Thus, we have studied device characteristics of low temperature a-Si:H TFT in terms of stability for driving electrophoretic display.

1. Introduction

In order to fabricate the flexible display, the flexible sheets such as plastic or stainless steel foil were developed as a substrate material [1-3]. A stainless steel has more advantages than other flexible substrates composed of organic materials in terms of process stability at high temperature, no thermal shrinkage, no water absorption and good competitive price.

We have developed various flexible displays using electrophoretic display (EPD) mode since 2005 [4-7]. The reflective property of EPD mode allows us to choose the opaque stainless steel substrate. However, it is needed to use organic layer in order to insulate between stainless steel substrate and thin-film transistor (TFT). Characteristic requirements of insulating materials are elasticity for flexible body, planarization of stainless steel surface, and the low dielectric constant. An organic material used TFT-LCD factory meets these characteristics, but there is a temperature limit on CVD process such as silicon nitride (SiNx), gate dielectric, and hydrogenated amorphous silicon (a-Si:H) after forming organic insulating material. In this respect, various prototypes were developed and exhibited at the journal and conference, but low TFT stability caused by low temperature process still remained an issue for mass production. In this paper, we discuss the stability of TFT on stainless steel substrate fabricated at low temperature CVD

2. Experimental

Figure 1 shows device structure of a-Si:H TFT on a stainless steel substrate. This structure is no difference from the conventional TFT except the conducting substrate and the insulating material on it. For approaching lightly, we adopt organic insulating material as a barrier which has been used in conventional LCD process. The organic insulating material was also used for improving the surface roughness of stainless steel. After forming the organic layer on stainless steel, a-Si TFT was fabricated at a CVD temperature of Max. 250℃ which is the process temperature of organic material as well.

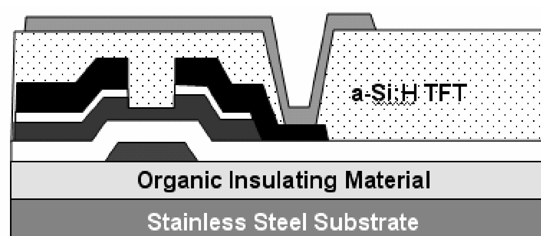

Fig. 1. Device structure of a-Si:H TFT on stainless steel substrate.

In order to compare device characteristics, we fabricated low temperature TFTs by changing the process temperature of SiNx and a-Si:H deposition at 250℃, 200℃, 150℃ on stainless steel substrate with

organic layer, and conventional TFT on glass substrate without organic insulating material.

3. Results and discussion

Figure 2 compares device characteristics of a-Si:H TFT depending on the CVD process temperature of 150℃, 200℃, 250℃ with conventional TFT, then each graph was measured at drain voltage (Vd) of 10V. Although on-currents of low temperature TFT related to field effect mobility are lower than that of conventional TFT, but device characteristics are enough for fabricating active matrix device to drive EPD.

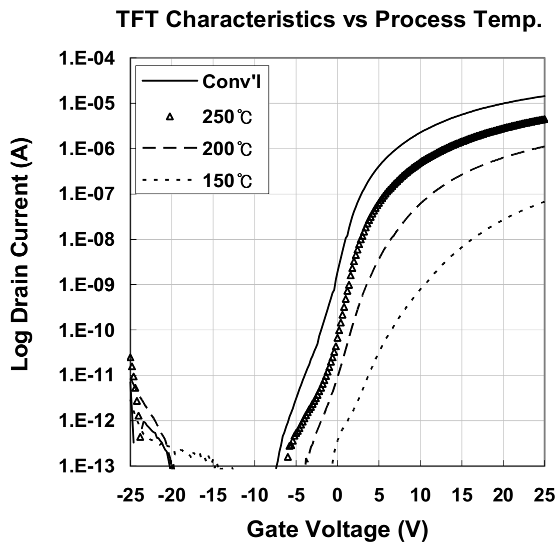

Fig. 2. Device characteristics of a-Si:H TFT depending on CVD temperature.

	Device	Conv'l	250℃	200℃	150℃	unit
Parameter	Ueff	0.60	0.22	0.01	0.0002	cm^2/Vs
	Vth	0.5	1.1	1.5	1.9	V
	S.S	0.98	0.55	0.62	0.68	V/dec
	Ion	0.58	0.38	0.01	0.0001	uA

Ion @ Vd=1V, Vg=20V

Table 1. Device parameters of a-Si:H TFT depending on CVD temperature.

Figure 3 shows bias thermal stress (BTS) characteristics of TFT by CVD temperature variation. For each device, drain current was measured before and after gate bias of ±30V at 60℃ condition. Variation range of negative BTS is between 0V ~ 0.6V, while that of positive BTS is between 1.7V ~ 3.4V. It is indicated that positive bias has a more influence on device characteristics than negative bias, and device fabricated at 250℃ has a minimum influence by gate bias. These are summarized in Table 2.

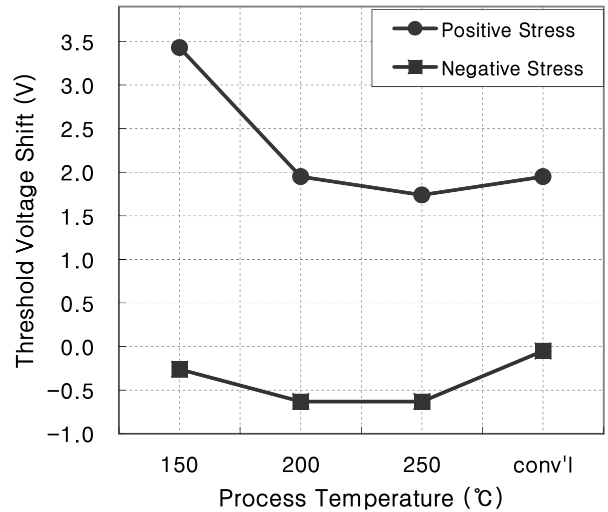

Fig. 3. BTS characteristics of TFT by CVD temperature variation.

Temp.	Condition	Vth	Shift		Total Shift
150℃	Initial	11.0	Nega Shift	**0.3**	3.7
	Nega30V	10.7			
	Initial	11.0	Posi. Shift	**3.4**	
	Posi30V	14.4			
200℃	Initial	5.5	Nega Shift	**0.6**	2.6
	Nega30V	4.9			
	Initial	5.5	Posi. Shift	**2.0**	
	Posi30V	7.5			
250℃	Initial	2.4	Nega Shift	**0.6**	2.3
	Nega30V	1.8			
	Initial	2.2	Posi. Shift	**1.7**	
	Posi30V	3.9			
Conv'l	Initial	1.2	Nega Shift	**0.0**	1.9
	Nega30V	1.2			
	Initial	0.7	Posi. Shift	**1.9**	
	Posi30V	2.6			

Table 2. BTS parameters of TFT by CVD temperature variation.

Although current levels of low temperature TFT are little bit low, we are able to get over it by adjusting

TFT dimension. Furthermore, there is no aperture ratio issue because we applied this TFT for the reflective type EPD.

For performance verification of low temperature TFT, U type dual TFT in one pixel was applied to conventional design rules with W/L of 80/5 and storage capacitor of 1.88pF. And, one simulated pixel voltage for the 250℃ TFT results in reaching 95% voltage charging within 13.9 ㎲ as shown in Figure 4.

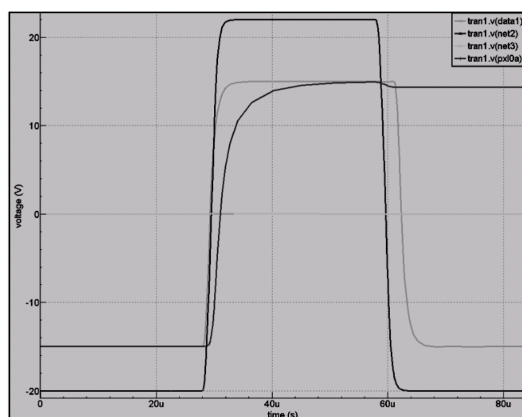

Fig. 4. The one pixel charging simulation using 250℃ TFT.

4. Summary

We developed a-Si:H TFT on stainless steel for the flexible display. In spite of low CVD temperature process for using organic insulating material on stainless steel substrate, we achieved relatively good TFT characteristics with keeping its bias stress stability. These performance and stability of low temperature TFT were enough to manufacture flexible display backplane, particularly for flexible EPD application

5. References

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