Hot Carrier Reliability of Short Channel (L=1.5μm) P-type Low Temperature poly-Si TFT

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Abstract

We have investigated the reliability of short channel (L=1.5μm) p-type ELA poly-Si TFTs under hot carrier stress. Threshold voltage of short channel TFT was significantly more shifted to positive direction than that of long channel TFT under the same stress. This result may be attributed to electron trapping at the interface between poly-Si film and gate oxide layer.

1. Introduction

Recently, low temperature poly-Si thin film transistors (LTPS TFTs) have attracted a considerable attention for active matrix organic light emitting diode (AMOLED) in the pixel switching and peripheral circuit [1], [2]. The operation speed of pixel transistor and peripheral circuit must be higher as the resolution of display increases. The short channel poly-Si TFT is required for high resolution display due to its high current driving ability. However, the reliability of short channel poly-Si TFTs is critical issue when the channel length is decreased [3]. It has been reported that the stability of polysilicon TFTs is poorer than that of single crystalline silicon MOSFETs after electrical stress [4].

The poor stability of poly-Si TFTs is due to the high density of in-grain and grain boundary defects besides interface state between the gate oxide and polysilicon film. Most previous works refer to the stability of poly-Si TFT have been mainly focused on long channel device. However, the degradation of short channel p-type poly-Si TFT, especially under the hot carrier stress, has been scarcely reported.

And degradation phenomenon of short channel Poly-Si TFT caused by the low gate and drain voltage is mainly originated in hot-carrier stress. Also, the hot carrier effects become increasingly important as the channel length becomes smaller, especially less than 2μm.

The purpose of our work is to investigate the electrical characteristic of short channel p-type ELA poly-Si TFT under the hot carrier stress. The relatively large positive shift of threshold voltage in short channel ELA poly-Si TFT was observed after hot carrier stress (100 seconds). This is due to the electron trapping, which was occurred by low gate-high drain bias condition, mainly at the interface near the drain junction. Reduction of leakage current in LTPS TFTs was also observed from the hot carrier stress.

2. Experimental

Top-gate p-channel poly-Si TFTs were fabricated using a conventional Excimer Laser Annealing (ELA) as shown in Fig.1 (a). At first, amorphous silicon films were deposited on the buffer oxide by Plasma Enhanced Chemical Vapor Deposition (PECVD). Typical excimer laser annealing (wavelength = 308nm) was utilized to crystallize the amorphous silicon film for a low temperature process followed by polysilicon active area patterning. A gate oxide (SiO_2, 80nm thick) and an interposed silicon nitride (SiN_x, 20nm thick) film were sequentially deposited in order to prevent the incorporation of mobile ions into the SiO_2 gate insulator [5]. The p+ regions were created by ion doping.

A gate metal was then formed and followed by doping in a p+ regions. A dielectric interlayer was deposited by PECVD. Sequentially, dopant activation was carried out thermally. Contact holes were formed, and a source / drain metal was deposited and patterned. A passivation layer was deposited and patterned to complete the fabrication process. Cross Section view of poly-Si TFTs are shown in Figure. 1(b) for SiO_2/SiNx double gate insulators.

In order to investigate the stability of polysilicon TFTs under low gate and high drain voltage stress, transistor with threshold voltage about V_{TH} = -1V ~ -2V were subjected to electrical stress under V_{GS} = (V_{TH}-1)V, V_{DS} = -20V for 100 seconds.

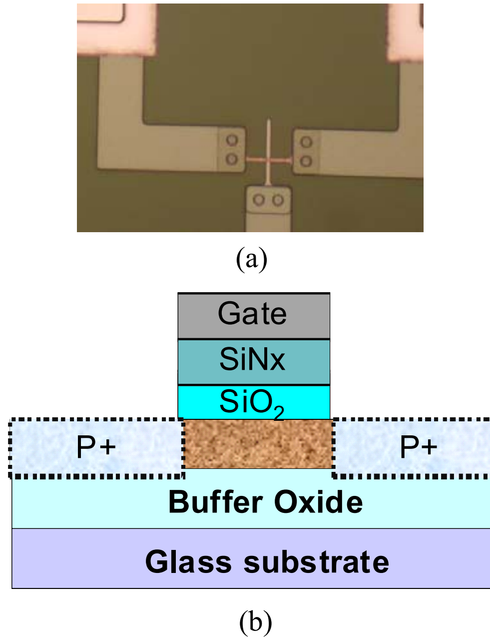
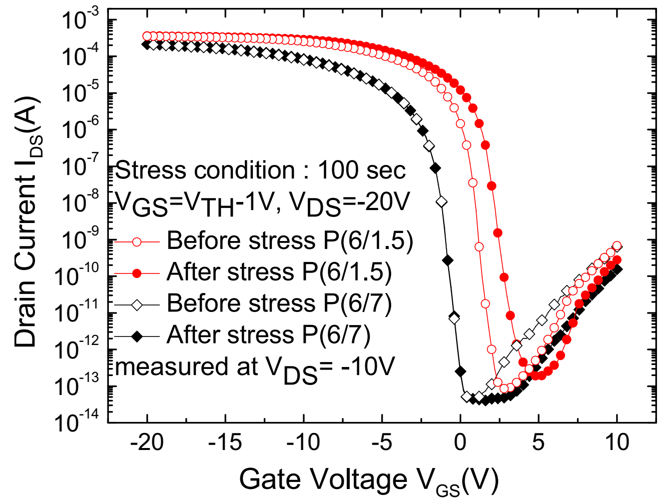


Figure. 1 (a) Plane view of fabricated ELA poly-Si TFT on the glass substrate (b) Cross Section view of poly-Si TFTs showing SiO_2/SiNx Double layer structures.

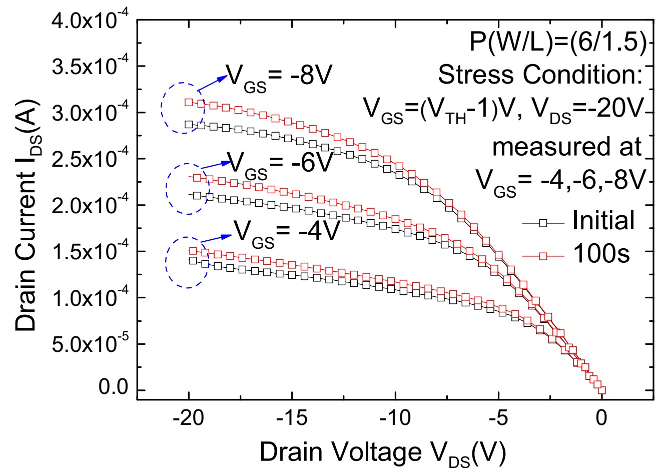
3. Results and discussion

We have measured transfer characteristics and threshold voltage of excimer laser annealing (ELA) poly-Si TFT with hot carrier stress according to stress times as shown in Figure. 1 (a), (b). We have applied a gate bias V_{GS} = (V_{TH}-1)V and drain bias V_{DS} = -20V to p-type ELA poly-Si TFT for 100 seconds in order to investigate an effect of the hot carrier stress on the transfer characteristic of the ELA poly-Si TFT.

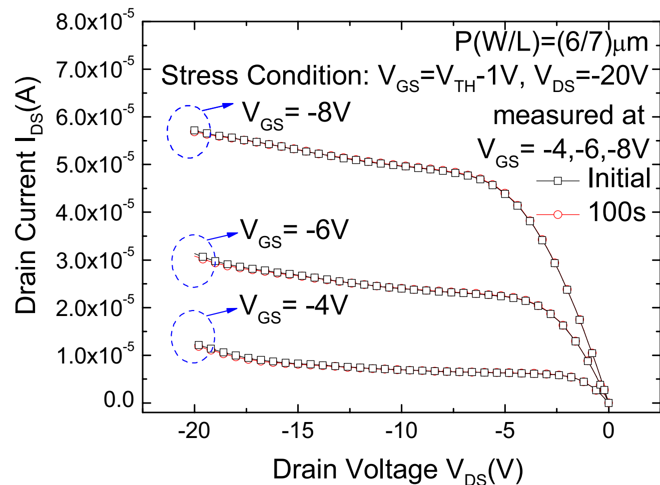
The transfer and output characteristics, measured before and after stress for 100 seconds are shown in Figure. 2. Relatively large V_{TH} shift of short channel TFT (L=1.5um) was occurred in the after stress transfer characteristic. And the drain current was increased at high V_{DS} after the bias stress in the output characteristic of short channel device (L=1.5um) whereas that of long channel device (L=7um) was scarcely changed. This means that avalanche induced short channel effect was occurred during hot carrier stress. It is known that kink current was originated from impact ionization near the drain junction [6].



(a)



(b)



(c)

Figure. 2 (a) Transfer characteristic and (b), (c) Output characteristic of ELA poly-Si TFT according to the hot carrier stress time (V_{GS} = V_{TH} -1V, V_{DS}= -20V, 100s) with various channel length.

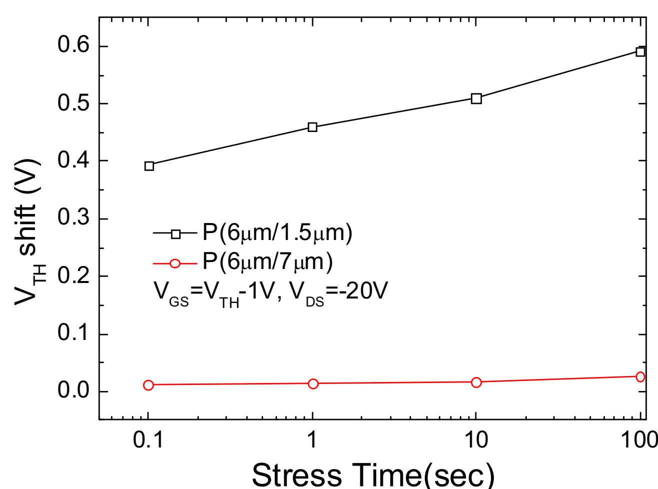


Figure. 3 Threshold voltage shift of ELA poly-Si TFT according to the hot carrier stress time (V_{GS} = V_{TH} -1V, V_{DS}= -20V, 100s) with various channel length. The threshold voltage of short channel device was significantly changed after hot carrier stress whereas that of long channel device was rarely altered.

As shown in Figure. 3, threshold voltage of ELA poly-Si TFTs with a various channel length was extracted as a function of stress time under hot carrier stress (V_{GS} = V_{TH}-1V, V_{DS} = -20V). After the hot carrier stress, the threshold voltage of ELA poly-Si TFT with L = 1.5μm was decreased by 0.59V (from -0.58 V to 0V at V_{DS} = -0.1V), whereas that of device with L = 7μm was reduced by only 0.02V (from -1.93 V to -1.90 V at V_{DS} = -0.1V).

This result was occurred due to the difference of proportion for the length of damaged region divided by an each channel length. Because the hot electron trapping was occurred into the gate oxide which increases the interface state densities at the gate oxide/poly-Si interface by the hot carrier stress, hole charges induced at the channel layer near drain junction.

Due to the existence of trapped electron charges, negative gate voltage could be effectively applied compared to non-damaged devices. For these reasons, the threshold voltage shift of short channel TFT showed a relatively larger value than that of long channel TFT as shown in Figure. 3.

And a proportion of damaged region (electron trapping occurred) in the total channel length was increased with a shorter channel length TFT, because the short channel device gains a higher effective electric field than that of long channel device, as shown in Figure 4. Therefore the effective channel length more seemed to be shortened and mobility appeared to be slightly increased in the short channel TFT.

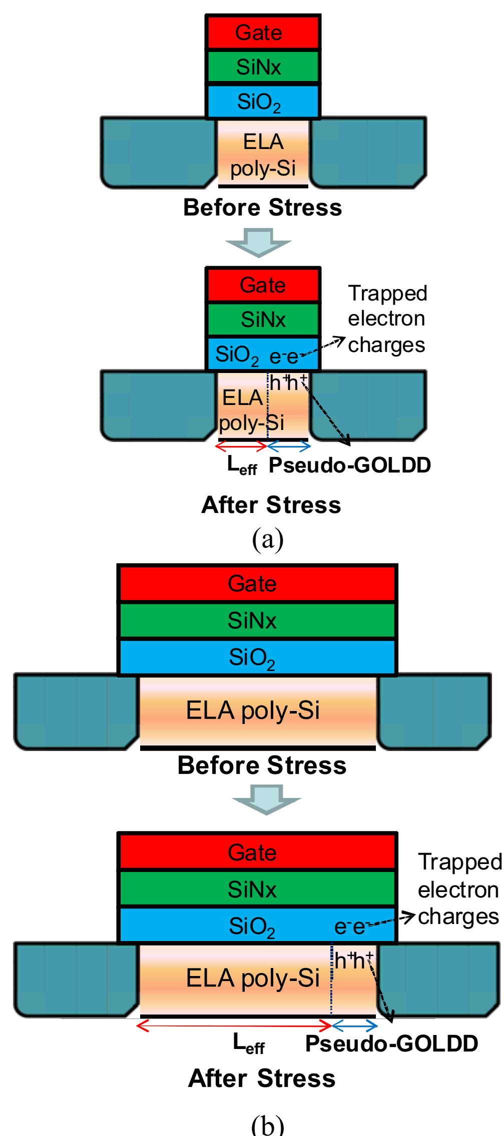


Figure. 4 Pseudo-LDD Model with the channel length dependence. (a) Short Channel, (b) Long Channel.

And Figure. 2 (a) also shows that the leakage current of each ELA poly-Si TFT was decreased with a constant bias stress for 100 seconds. Even on-current was slightly increased compared with that of device before hot carrier stress. The leakage current was dramatically decreased after the initial electrical stressing for 0.1s. And the leakage current of TFTs was saturated after hot carrier stress. During the initial stress, generated electrons were trapped into the gate oxide near the drain junction. Hole charges were

generated in the channel region correspond to the initially trapped electron charges. It was worked as a gate overlapped lightly doped drain (GOLDD) in the device [7]. The trapped electrons in the gate oxide layer relieve the electric field near the drain junction, which leads to the reduction of leakage current under the hot carrier stress.

4. Summary

We have investigated the stability of short channel p-type ELA poly-Si TFT under hot carrier stress. Threshold voltage of the short channel TFT was considerably moved to the positive direction under the stress, whereas the threshold voltage of a long channel was rarely moved to the positive direction. This positive shift of threshold voltage in the short channel TFT may be due to the electron trapping at the interface near drain junction. Moreover, the effective channel length in the short channel TFT was more reduced than that of long channel TFT.

5. References

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