Dry Etching Process for the Fabrication of Transparent InGaZnO TFTs

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Abstract

We proposed the dry etching process recipe for the fabrication of In-Ga-Zn-O (IGZO)-based oxide TFTs, in which the etching behaviors of IGZO films were systematically investigated when the etching gas mixtures and their mixing ratios were varied. Good device characteristics of the fabricated TFT were successfully confirmed.

1. Introduction

Oxide-based thin-film transistors (TFTs) have great potentials for realizing future information-related applications, such as transparent displays [1] and flexible electronic devices [2], owing to their transparency in visible range and compatibility to lower-temperature process. Amorphous In-Ga-Zn-O (IGZO) has been reported to be one of the most promising materials to provide a semiconducting channel for the TFTs [3-5], because it is free of grain boundaries in channel regions, which may cause some degradation of the TFT stability and uniformity, unlike another candidate of ZnO. Although the previously reported TFT using IGZO channels have shown good performances, the sizes of such devices are still relatively big. It relates to the fact that the IGZO channels have been generally patterned by chemical wet etching method so far. Eventually, the device structure and size are limited by the isotropic etching behavior and poor etching selectivity between IGZO and other oxide materials of the gate insulators and/or electrodes of TFT. However, such advanced applications as high-resolution backplane for the active-matrix displays and high-performance transparent integrated circuits require smaller device sizes and better roll-off properties of TFTs. Therefore, it is important and urgent to develop the patterning methods using dry etching techniques for the IGZO. So far, there were few reports on the dry etching behaviors of amorphous IGZO for the TFT applications. The first object of this study is to systematically investigate the dry etching characteristics of IGZO by varying the etching gas mixtures and their mixing ratios. The second object of this study is to provide the optimized patterning recipe when the IGZO and ITO are employed as an active channel and source/drain (S/D) electrodes, respectively. Then, using the obtained pattering recipe, top-gate IGZO TFT was fabricated and characterized.

2. Experimental

In this study, we used the etching apparatus using high-density helicon plasma (LSE-800, manufactured by Leed), which provides an ultimate high-density helicon wave plasma (e.g., $1x10^{11}/cm^3$ at the input power of 500 W and the chamber pressure of 2 mTorr). The details of system configuration and structure can be referred in another publication [6]. For the investigation on the etching rates of IGZO and ITO films, they were prepared on Si or glass substrate by sputtering method. The helicon source and RF chuck were operated at 60 MHz and 13.56 MHz, respectively. The temperature of the sample holder was controlled by He gas and held at 35°C. The etching parameters of RF main power, RF bias power, and chamber pressure were fixed at 800 W, 600 W, and 5 mTorr, respectively. In this work, gas mixtures of Ar/Cl_2 and Ar/CF_4, and $Ar/Cl_2/CF_4$ with various mixing ratios were employed for the dry etching of IGZO and ITO films, where the etch rates (ER) and etch selectivities (ES) in given gas mixtures were investigated.

3. Dry etching behaviors of IGZO and ITO

Figure 1 shows the ER's of IGZO and ITO as a function of gas mixing ratio of Ar/Cl_2 and Ar/CF_4. With the increase of Cl_2 ratio from 10 to 60%, the

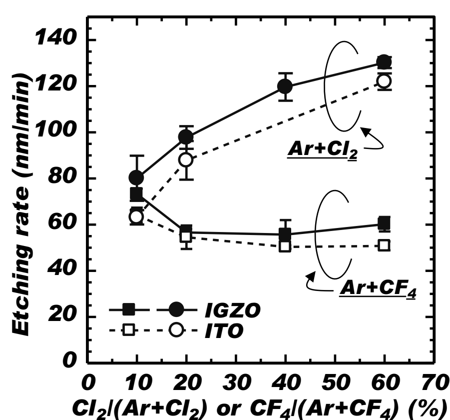

Fig. 1. Etch rates of IGZO and ITO in Ar/Cl_2 and Ar/CF_4 etching gas mixtures.

ER's of IGZO and ITO increased from 80 to 130 nm/min and from 60 to 120 nm/min, respectively. On the contrary, in the gas mixture of Ar/CF_4, the ER's of IGZO and ITO did not increase with the increase of CF_4 and appeared to be saturated around 60 nm/min. It can be found that Cl_2^+ ions in the Ar/Cl_2 gas mixtures play a main role for increasing the chemical reactivity and/or physical sputtering effect for the dry etching of IGZO and ITO.

To elucidate the effect of CF_4 for the etching process, the Ar/Cl_2/CF_4 gas mixtures were applied, in which the mixing contents of Cl_2 and CF_4 were set to be the same, as shown in Fig. 2. As can be seen in figure, when the mixing ratio of CF_4 was varied to more than 20%, the ER's of IGZO and ITO were observed to be saturated and inversely reduced, respectively. It is interesting to note that we can improve the ER's of both films by blending some

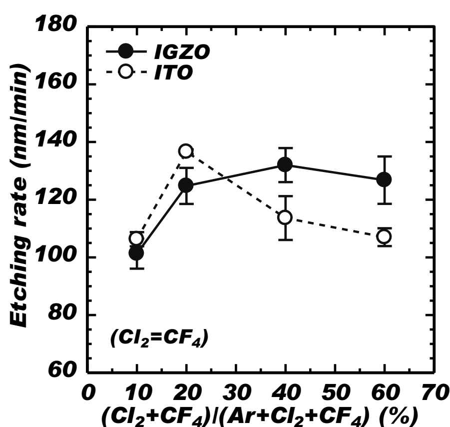

Fig. 2. Etch rates of IGZO and ITO in Ar/Cl_2/CF_4 (Cl_2=CF_4) etch gas mixtures.

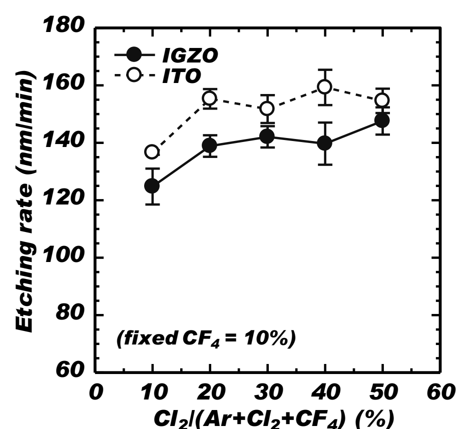

Fig. 3. Etch rates of IGZO and ITO in Ar/Cl_2/CF_4 (fixed CF_4) etch gas mixtures.

fixed content (10%) of CF_4 in the Ar/Cl_2/CF_4 mixtures, as shown in Fig. 3. In these conditions, the ER's of IGZO and ITO were obtained in the range from 125 to 145 nm/min and from 135 to 160 nm/min, respectively, which were larger values than those for the conditions using single reactive gas of Cl_2. These results suggest that the addition of a small amount of CF_4 into the Ar/Cl_2 gas mixtures enhanced the ER's of oxide films due to an increase in ion-assisted desorption. On the other hand, when it comes to the ES between IGZO and ITO, a sufficiently large value could not be obtained in any etching gas mixture employed in this study, which seems to be resulted from the fact that two oxides include common or similar ingredients.

From the obtained results and discussions, we propose the two-step etching recipe for the IGZO channel layer formed on the ITO electrodes to fabricate the TFTs by exploiting the differences of ER's of both films between in the Ar/Cl_2 and in the Ar/CF_4 mixtures. This etching recipe, as presented in Fig. 4, was so designed to effectively pattern the IGZO channel layer, minimizing the damage to ITO electrodes. At the first step, the IGZO active layer was patterned by using the Ar/Cl_2/CF_4 (80/10/10) etching gas mixtures with a higher etch rate in a shorter time, in which a very thin layer of IGZO could be remained for the protection of ITO. Then, at the second step, the remained IGZO was thoroughly removed by using the Ar/CF_4 (80/20) with a slower etch rate. Two beneficial features can be expected in employing this recipe. One is to minimize the effect of plasma-induced damages to the active channel region of IGZO by minimizing the etching time of main patterning

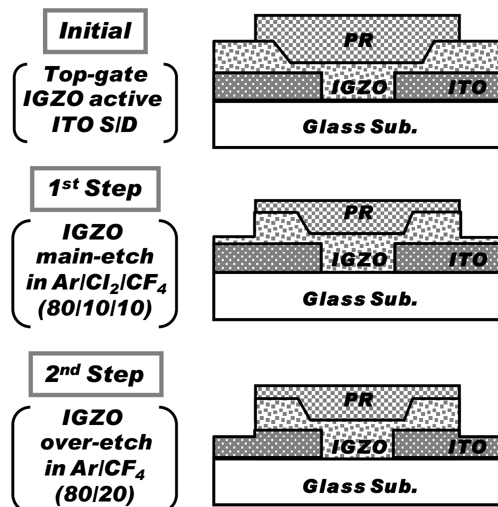

Fig. 4. Dry etch process recipe for the top-gate IGZO-TFT.

process. The other is to carefully control the surface roughness of exposed ITO by reducing the etch rate during the over-etch process of IGZO, which is important because that the ITO was connected to the electrode pad via Al interconnection in full fabrication process for the TFT. Figure 5 shows the typical photograph of the resultant IGZO channel patterned on the ITO S/D electrodes.

4. Fabrication and Characterization of IGZO TFT using Dry Etching Method

The top-gate oxide TFT was fabricated by using the proposed etch recipe, where Al, SiO_2, IGZO, and ITO films were used as a gate electrode, a gate insulator, a channel layer, and S/D electrodes, respectively. The device fabrication procedures are as follows. First, the ITO layer was patterned to form S/D electrodes using wet etching process. Then, a 25-nm-thick IGZO was deposited by rf magnetron sputtering method at room temperature using Ar/O_2 (85/15) gas mixtures under

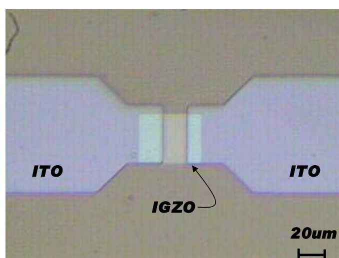

Fig. 5. Photograph of the IGZO pattern formed by dry etching on the ITO.

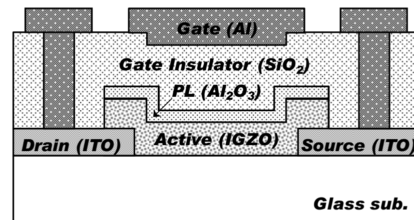

Fig. 6. Schematic cross-sectional diagram of the fabricated top-gate IGZO-TFT.

the working pressure of 1~5 mTorr. The target composition of In:Ga:Zn was 1:1:1. Prior to the preparation of gate insulator, a thin Al_2O_3 layer was deposited on IGZO by PEALD method at 150^oC, which could be expected to act as a protection layer for protecting IGZO channel from the following lithography process using several organic solvents. For the patterning of IGZO channel area, the dry etching recipe developed in this work (as shown in Fig. 4) was employed, in which the etching time was carefully determined by considering the ER's of IGZO and ITO in given process conditions. On the patterned IGZO active channel layer, the gate insulator of SiO_2 with the thickness of 100 nm was formed by ionized physical vapor deposition method, which was verified to have a sufficiently low leakage current of approximately 10^{-12} A at the application of 30 V [7]. Finally, Al gate electrode was deposited by sputtering method and patterned using a wet etchant after via contacts on the S/D electrodes were formed. Figure 6 shows a schematic cross-sectional diagram of the TFT.

Figure 7 (a) shows the output characteristics (I_D-V_{DS}) of the fabricated IGZO-TFT with the gate width (W)/length (L) of 40 um/20 um when the gate voltages were varied to 0, 5, 10, 15 V, which showed good saturation behaviors even at high drain voltage. Ohmic contacts between the ITO S/D electrodes and IGZO channel were observed to be well formed. Moreover, undesirable increase of contact resistance between the ITO and Al interconnection was not detected. The transfer characteristics (I_D-V_{GS}) and the gate leakage currents of the fabricated TFT were also measured at a range of drain voltage from 0.5 to 15.5 V, as shown in Fig. 7(b). The field effect mobility, the threshold voltage, and the subthreshold swing (S value) were estimated to be approximately 30.9 cm^2/Vs, 8.5 V, and 0.47, respectively. The obtained values are comparable to those for the device fabricated by the conventional wet etching method. The off currents were as low as 10^{-10} A and the ratio of on/off drain currents in transfer characteristics was

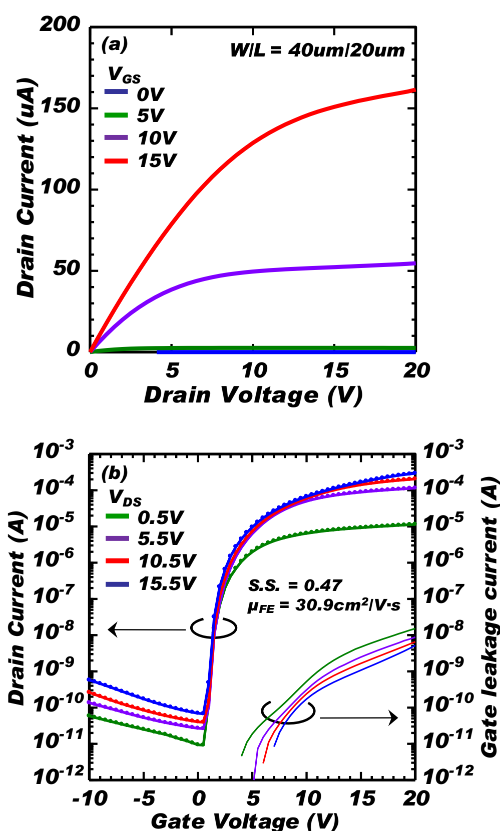

Fig. 7. (a) Output and (b) transfer characteristics of the fabricated IGZO-TFT using a dry etching method.

more than 10^6. These results suggest that the dry etching recipe proposed in this work provided sound pattern shapes of IGZO channel layer without any residue and any damage caused during the plasma-induced process. Therefore, it can be concluded that the IGZO-TFT was successfully fabricated by employing the developed dry etching process.

5. Summary

An optimized dry etching process was proposed for realizing the top-gate IGZO-TFTs by carefully investigating the etching behaviors of IGZO in various gas mixtures. The recipe was composed of the first main-etch process of IGZO using $Ar/Cl_2/CF_4$ (80/10/10) and the second over-etch process using Ar/CF_4 (80/20). Good device characteristics of the fabricated TFT by employing this recipe were well confirmed. The dry etching techniques can be effectively employed for the next-generation high-performance large-area transparent and/or flexible electronic devices.

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