# A New Voltage Driving Method for Large Size and High Resolution AMOLED Displays with a-Si:H Backplane.

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## Abstract

We propose a novel n-type a-Si:H TFT pixel circuit which is proper to AMOLED display for the large size and high resolution. Proposed pixel circuit will be suit to panel for the high resolution because of different threshold sampling method. Driving method of proposed pixel circuit is very simple like an AMLCD. Our simulation indicates that the proposed pixel circuit can compensate the Vth shift and IR rising of power line so that provide better quality image.

## 1. Introduction

There is no question that Active Matrix Organic Light Emitting Diode (AMOLED) TV will be commercialized. A-Si:H has drawn much attention for the candidate of AMOLED TV Backplane. Because of using the existing infrastructure, AM-LCD companies have merit to low investment and manufacturing cost. But there is a serious defect to use an a-Si:H TFT as a reliable backplane for AMOLEDs. It is the luminance deterioration and image stacking issues as time goes by. That is an unstable characteristics induced from DC gate bias of driving TFT in the pixel circuit. The causes of the unstable characteristics have been investigated by two mechanisms. One is creation of metastable state on a-Si:H and the other is charge trapping in the silicon nitride gate insulator [1]. Those mechanisms give rise to the Vth Shift of an a-Si:H TFT. To solve the Vth shift problem, various pixel circuits was introduced [2-4]. Among them voltage compensation method is best application for the large size and high resolution AMOLED panels [5]. Recently negative bias methods have been reported to recovering the Vth shift of driving TFT in the pixel. But complex driving method for the gate node of the driving TFT with negative voltage (Symmetric DC Voltage) is very difficult to using large size AMOLED panels [6]. Figure 1 show comparison of the Vth Sampling time of the conventional n-type TFT compensation circuit (Vth is sampled by discharging method) and p-type TFT compensation circuit (Vth is sampled by charging method) with Pixel Per Inch (PPI).

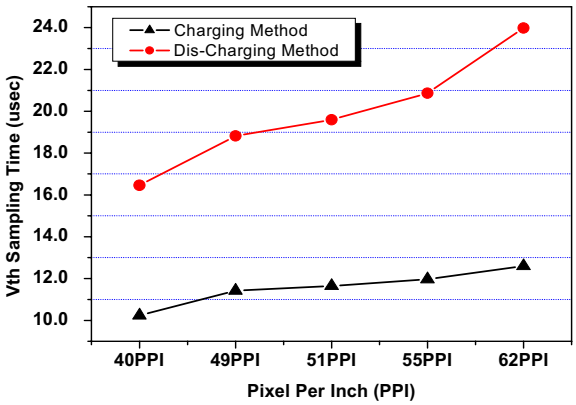


Figure 1, Comparison of Vth Sampling time with p-type (Charging) and n-type compensation method (Discharging).

Because channel length becomes small as PPI increasing; discharging method of the Vth Sampling time is seriously affected. Simulation results show that charging method has advantage for the AMOLED panel driving of more than higher 62PPI. Moreover the Vth shift compensation circuit of n-type a-Si:H TFT has longer program time which consists of the Vth sampling and compensation period so that prior voltage driving method is difficult for implementation in the high resolution AMOLED panels. So we have studied charging method and simple driving using n-type TFT. Proposed novel pixel circuit has charging and simple driving method and a full line time to the Vth sampling like an AMLCD. Besides the proposed pixel circuit has scale-down factor by ratio of two capacitors in the pixel circuit so that it should be useful for high resolution gray implementation of the high efficient Organic Light Emitting Devices.

## 2. Proposed Pixel Circuit

We proposed a new n-type TFT pixel circuit employing the threshold voltage detection scheme by charging method. Figure 2 shows the block diagram of proposed pixel circuit. Proposed Pixel circuit is composed of n-type 4 TFTs (DR,

SW1, Sw2 and SW3) and 2 Capacitors, and 2 Gate Lines (Scan1, Scan2) and 1 Data line and Power Lines.

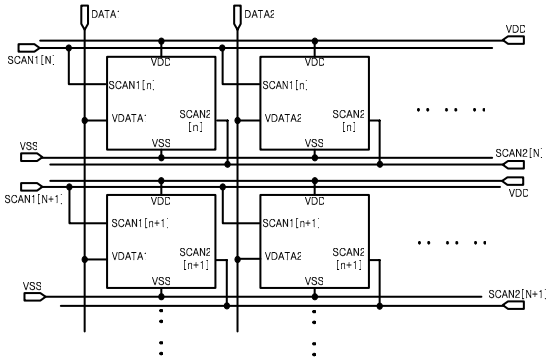


Figure 2, Block diagram of proposed pixel circuit array.

Driving method of proposed pixel circuit is different with prior introduced n-type TFT voltage compensation scheme, which driving was divided into minimum 3 states (Initial, Vth Sensing, and Program). But Proposed Pixel circuit has only Program state. So that proposed driving method is same as conventional 2T1C voltage driving circuit.

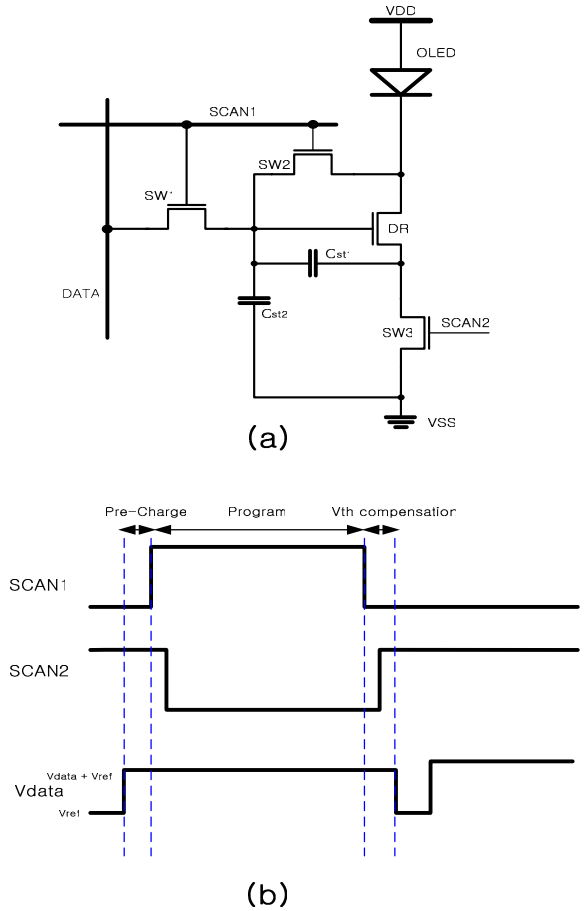


Figure 3, Proposed pixel circuit. (a) Circuit diagram, (b) Timing diagram

Figure 3 show the proposed pixel circuit and timing diagram. The operation of pre-charge period, The Data line is applied to Vref+Vdata (Vref > VDD). In the period of program, SCAN1 becomes high to SW1 & SW2 TFT Turn on so that drain node of Driving TFT is biased with same gate node voltage (Diode connection). Since Vref voltage is higher than VDD, OLED is reversely biased so current flow is prevented from the OLED. In order to preventing the current from data line to VSS line, SCAN2 is applied low to SW3 TFT turn off simultaneously. During program, Source node of Driving TFT is charged to Vref+Vdata-Vth from VSS Voltage resulting from the gate and drain voltage are same Vref+Vdata. Consequently Cst1 capacitor stores the threshold voltage of Driving TFT. In the period of Vth compensation, SCAN1 is applied Low to Turn off SW1/ SW2 TFTs so that Gate node of Driving TFT is Floating State. At that time, SCAN2 Line is applied to high to turn on SW3 TFT. The source node voltage of DR TFT (Vref+Vdata-Vth) is discharged to VSS (if there is no IR Rising). Because of Capacitor's charge conservation characteristic, the gate node voltage will be changed. The changed voltage can describe below equation

$$V_g = \frac{C_{ST2}}{C_{ST1}+C_{ST2}}\cdot\left(V_{DATA}\right)+\frac{C_{ST1}}{C_{ST1}+C_{ST2}}\cdot\left(Vx+V_{TH}\right)$$
$$=\alpha\cdot\left(V_{DATA}\right)+\beta\cdot\left(Vx+V_{TH.}\right)$$
$$\left(\therefore \alpha=\frac{C_{ST2}}{C_{ST1}+C_{ST2}} \quad \beta=\frac{C_{ST1}}{C_{ST1}+C_{ST2}}\right)$$

Here Cst1 and Cst2 are internal capacitors of pixel circuit. $V_{TH}$ is the threshold voltage of driving TFT. Vx is the source voltage of driving TFT. If the value of Cst1 is much larger than that of Cst2, we can re-write as below.

$$\beta\approx 1 \quad (\because C_{ST1} >> C_{ST2})$$
$$V_g = \frac{C_{ST\,2}}{C_{ST\,1}}\cdot\left(V_{DATA}\right)+V_X+V_{TH}$$

This equation verifies the compensation of the driving TFT's Vth and IR rising. Proposed pixel circuit shown that the Vdata is scaled down as ratio of Cst1 and Cst2.

The $I_{OLED}$ of the proposed pixel circuit is represented by following equation

$$I_{OLED} = \frac{k}{2}\cdot(Vgs-V_{TH})^2$$
$$=\frac{k}{2}\cdot\left(\frac{C_{ST\,2}}{C_{ST\,1}}\cdot\left(V_{DATA}\right)+V_X+V_{TH}-V_X-V_{TH}\right)^2$$
$$=\frac{k}{2}\cdot\left(\frac{C_{ST\,2}}{C_{ST\,1}}\cdot\left(V_{DATA}\right)\right)^2$$

Here k is $\mu\cdot C_{OX}\cdot W/L$. Therefore proposed pixel circuit is independent of Vth and IR rising from VSS power line.

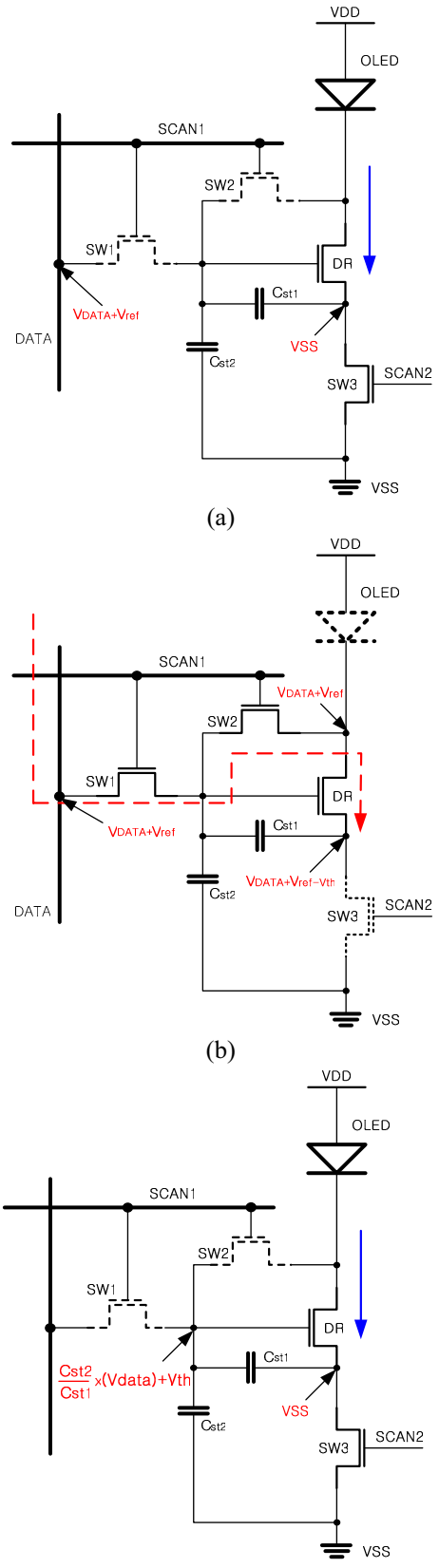


Figure 4, Operations of proposed pixel circuit. (a) Pre-charge period, (b) Program period, (c) Vth compensation period.

## 3. Simulation results

In order to verify the proposed circuit performance, we carried out simulation using SMART Spice TFT Model (RPI Level 35) [7]. Using TFT model library is a high temperature fabricated a-Si:H TFT model which has high immunity for the Vth shift relatively. Figure 5 shows the gate and source voltage of DR TFT in the proposed pixel circuit and Figure 6 shows the OLED output current with operation time. We performed transient simulation of the same data voltage is biased to the proposed pixels which have a different threshold voltage of driving TFT (1.7V and 2.7V (assume 58% shifted)). Figure 5 show the source nodes of DR TFT are charged up to approximately 16V and 17V within 10usec. In period C the source node voltages are discharged to VSS so that gate node voltages are scale down to 3.4V and 4.2V by ratio of Cst1 and Cst2.

This result proves that the Vth shifted of DR TFT is compensated. As shown in Figure 6, each proposed pixel circuits provide OLED current in 397.84nA and 378.36nA. In spite of difference 1V threshold voltage, The OLED error current only exist about 5% variation. These simulation results verify the ability of the Vth shift compensation successfully.

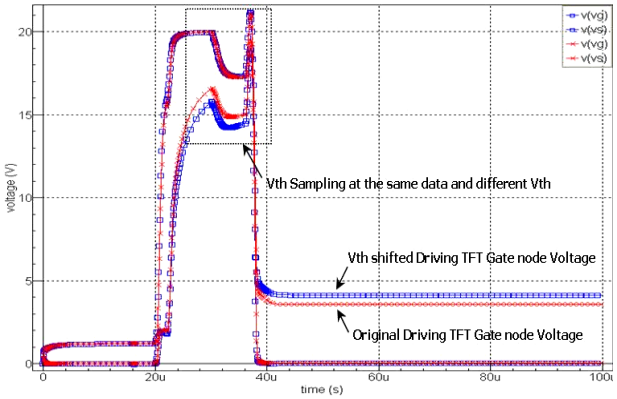


Figure 5, Simulation result of programmed voltage of proposed pixels

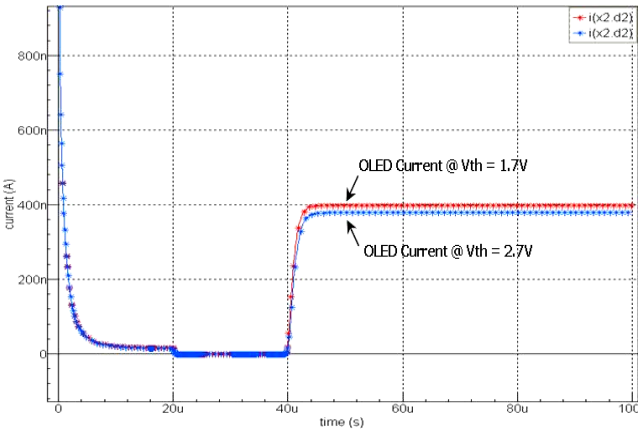


Figure 6, Simulation result of OLED current of proposed pixels

Proposed pixel circuit is going to fabricate in Test Pattern and we plan to measure the driving current the effects of the Vth shift as time goes by.

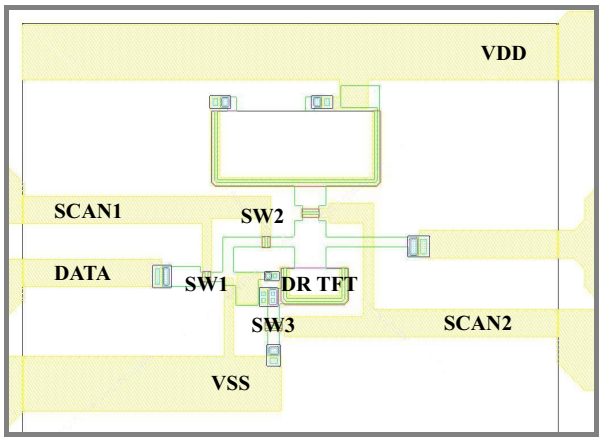


Figure 7, Layout of proposed pixel circuit.

## 4. Conclusions

The operation of the proposed pixel circuit is very simple like a conventional 2T1C scheme. Especially Vth sampling time of proposed pixel circuit has all the time of gate turn on time. So we can use longer program time than existing a-Si:H TFT based pixel circuits. And proposed pixel circuit can compensate the Vth shift and IR rising of power line so that provide better quality images. It will be the best merit for the large and high resolution AMOLED panel.

## 5. References

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