TFT-LCD Display Quality Improvement by the Adjustment of Gate Line Structure

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Too high stress of the bottom Mo layer of the gate line is thought to be the main reason for H-line mura. H-Line mura is eliminated effectively by changing the gate line metal structure from Mo/AlNd/Mo to AlNd/Mo. The new structure does not influence the panel's electrical characteristics.

1. Introduction:

The Mura is a sort of display defects, which shows display gray level non-uniformity on the display screen. A simple way to detect mura is to change the display pattern to black pattern or other low gray level pattern in the darkroom. Observing the display screen from different angles, various types of mura could be seen on the display screen along with various manufacturing flaws. In this paper, we have discussed the mechanism and solution of H-Line Mura.

2. Defect Mechanism Analysis:

Under gray scale 60, we find bright thin lines around the gate pad area, which is named as the H-Line mura. The H-Line mura is composed of some small white lines along the gate lines and just happened near the gate pad area whose width is less than 10cm.

A、Gate layer reflectance difference

During gate line forming process, we make use of three-layer structure, Mo/AlNd/Mo. This kind of structure could eliminate the pinhole phenomenon on the AlNd layer. Whereas the stress of bottom Mo layer around the glass edge becomes higher than that on the center of the glass for different thickness [1]. Therefore glass presents an uneven distortion after thin film process.

During the gate etching process, top Mo layer etching rate on the glass center is lower than that around the edge area. AlNd layer on the edge of the glass exposures more than that on the center of the glass as shown in Fig.1. The pixel reflection ratio difference occurs and arouses the H-Line mura.

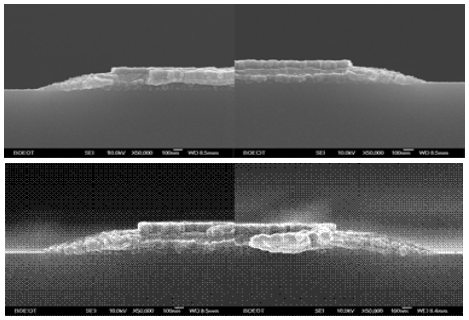

Fig.1 Centre area (up) & Edge area (down), Top Mo Layer Over etch SEM Image.

B、Gate Mask vs S/D Mask alignment difference

As to the Gate layer reflectance difference presumption, the stress of bottom Mo layer around the glass edge is higher than that on the center of the glass as shown in Fig.2. The distortion is caused by uneven local thin-film stress distribution on the glass. After gate etching process, glass stress decreases and turns out to be horizontal. Glass releases vertically stress. The closer it is to the glass edge, the greater the stress becomes [2].

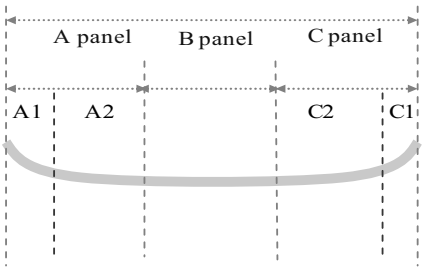

Fig.2 Glass Width (Gate Layer Deposition & Mask).

The S/D overlay shift of glass edge become too bigger than glass center as shown in Fig.3 is caused by stress difference after S/D (source and drain) mask process. Cgs non-uniformity also exists because of the offset difference between glass center and edge area. Fig.4 and Table.1 show the mask shift difference. The difference between the first data pad and the second data pad is 0.9μm.

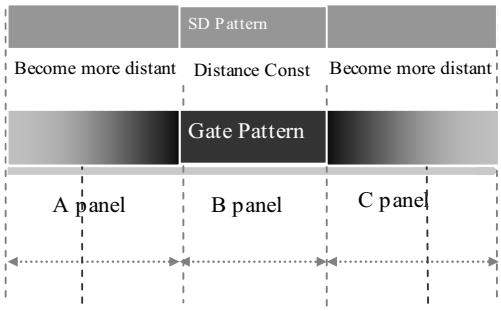

Fig.3 Glass Width (S/D Mask).

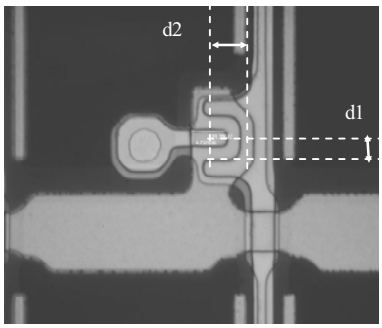

Fig.4 Cgs Measurement Pattern

Table.1 Cgs Measurement Real Data.

		Data Pad1 (μm)	Data Pad 2 (μm)	Data Pad3 (μm)	Data Pad4 (μm)
Bi Gate	D1	4.32	4.57	4.47	
	D2	12.60	12.25	12.64	
Tri Gate	D1	4.84	4.79	4.70	4.81
	D2	12.43	11.52	11.65	11.55

Considering ΔV_p = (Cgs / Ctotal) * ΔV_g, ΔV_p (Feedback Voltage) difference still exists and arouses LC (Liquid Crystal) layer voltage abnormal.

C、Feedback Voltage difference:

By the SEM (Scanning Electron Microscope) analysis as shown in Fig.5 and Fig.6, with the thickness increase of the bottom Mo layer, void area occurs at the gate line edge. This kind of phenomenon is also caused by Mo stress difference between the center and edge of

the glass. ΔCgs and ΔV_p difference occurs between the glass center and edge area.

As shown in Fig.5, it is the simulant result about ΔV_p. Presumption: Length (L) is 12.75μm, Gate thickness (h) is 3600 Å, α is 45 degree, x is a variable that reflects the size of void area. When x is equal to 1800Å, $\Delta(\Delta V_p)$ is 0.0219V, and the change rate of ΔV_p is 1.34%. When x is equal to 3600Å, $\Delta(\Delta V_p)$ is 0.0439V, and the change rate of ΔV_p is 2.67%. When x is equal to 7200Å, $\Delta(\Delta V_p)$ is 0.0878V, and the change rate of ΔV_p is 5.35%. The change rate of ΔV_p is more obvious with the increasing x value.

Table.2 Gate Distance Conversion & ΔC, ΔV_p Calculation.

x(Å)	0	360	720	1080	1440	1800	2160	2520	2880	3240	3600
ΔC%=ΔVp%	0.00%	0.27%	0.53%	0.80%	1.07%	1.34%	1.60%	1.87%	2.14%	2.41%	2.67%
Δ(ΔVp)(v)	0.0000	0.0044	0.0088	0.0132	0.0176	0.0219	0.0263	0.0307	0.0351	0.0395	0.0439

x(Å)	3960	4320	4680	5040	5400	5760	6120	6480	6840	7200
ΔC%=ΔVp%	2.94%	3.21%	3.47%	3.74%	4.01%	4.28%	4.54%	4.81%	5.08%	5.35%
Δ(ΔVp)(v)	0.0483	0.0527	0.0571	0.0615	0.0658	0.0702	0.0746	0.0790	0.0834	0.0878

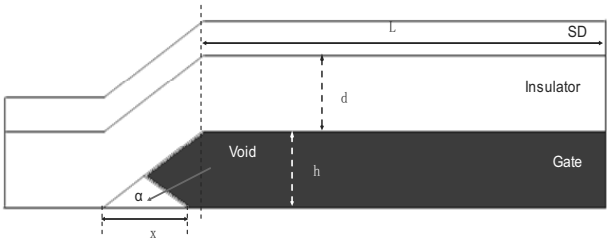

Fig.5 Void Sketch Map

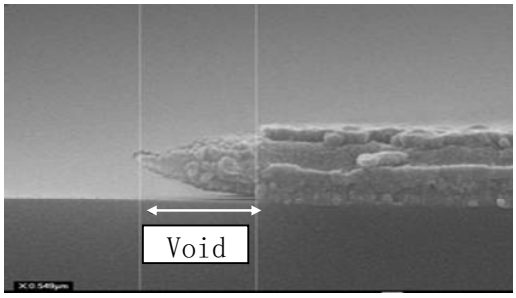

Fig.6 Void SEM Image.

3. Method and Effect:

All the mechanisms are based on the Mo layer non-uniform stress on the bottom Mo of the gate layer. We changed the three layer structure Mo/AlNd/Mo into two layers structure (bottom) AlNd/Mo (top) as shown in Fig.7. In the two-layer structure, when the top Mo layer becomes relatively thick, H-Line Mura still exists, which is caused by the galvanic corrosion phenomenon [4] [5]. If we decrease the Mo layer to 400Å, H-Line Mura disappeared. After annealing process, there's no resistance difference between Mo/AlNd/Mo and AlNd/Mo structure. AlNd/Mo structure has no influence on the product's electrical characteristic.

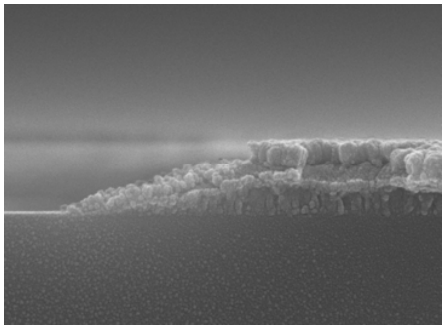

Fig.7 AlNd/Mo Structure SEM Image.

4. Conclusion:

By the adjustment of gate line structure, the structure is changed from the Mo/AlNd/Mo to the AlNd/Mo. It effectively reduces the H-Line Mura. During the mass inspection of products, there's no H-Line Mura occurs again. Two layers structure could effectively remove the H-Line Mura and improve the production yield.

5. Reference:

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