Organic field-effect transistors with step-edge structure

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Abstract

The organic field-effect transistors with step-edge structure were fabricated. Source and drain electrodes were obliquely deposited by vacuum evaporation. The step-edge of the gate electrode serve as a shadow mask, and the short channel is formed at the step-edge. The excellent device performances were obtained.

1. Introduction

Recently high performance electric and optoelectronic devices based on organic semiconductors have been demonstrated, such as OLED, thin-film transistors (TFT), and solar cells. These organic devices show promise for low-cost, large-area and flexible devices. In particular, display panels using OLED are expected for mobile electronic devices and excellent stability and high efficiency OLED have been reported. On the other hand, rapid progress of organic transistors has been made in recent years [1-3]. Furthermore, all-organic display devices are expected by combining the OLED with organic transistors [4-7], because organic transistors driving OLED are necessary to achieve flexible and large scale active-matrix-displays. To be practical, however, it is necessary to operate with a drive voltage as low as a few volts and have sufficient reliability. Conventional organic field-effect transistors (OFETs) have low-speed, low-power, and relatively high operational voltage mainly due to their low-mobility and high-resistivity.

From these points of view, we have proposed vertical-type OFETs with a short channel length [4-6]. In this paper, we proposed a step-edge vertical channel OFET (SVC-OFET) for achieving the short channel length by a simple fabrication procedure.

2. Experimental

The device structure and fabrication process are

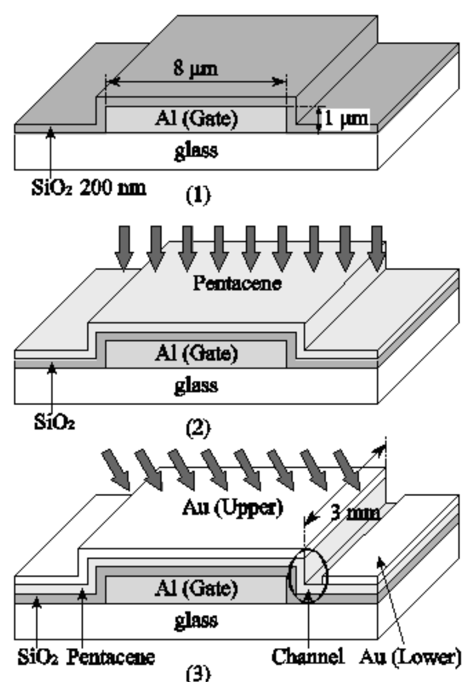


Fig. 1. Schematic views of the device structure and fabrication process.

shown schematically in Fig. 1 (1)-(3). First, Al gate electrodes lines (line width of 8 μm, thickness of 1 μm) were patterned on a glass substrate and covered with a 200 nm - thick SiO_2 film. Second, the pentacene thin film of 50 nm was deposited using vacuum evaporation technique at approximately $2x10^{-4}$ Pa. Finally, Au was deposited on the pentacene film by an incline vacuum evaporation technique to form the source and drain electrodes. The step-edge of the gate electrode serve as a shadow mask and the short channel is formed at the step-edge. The channel length corresponds to the thickness of the gate electrode and the channel length is controlled by choosing the thickness of Al gate electrode. OFETs with a short channel length around 1 μm have been realized.

The electrical characteristics were measured using semiconductor parameter analyzer (Agilent 4156C) in vacuum at room temperature.

As shown in Fig. 1 (3), SVC-OFET has an asymmetric structure concerning the source and drain electrodes. We call upper-source and lower-source depending on the electrical connection as a source or drain electrode. Figure 2 shows the SEM photograph around the step-edge region of SVC-OFET. In this case, the estimated gap between the upper and lower electrodes which corresponds to the channel length was approximately 1 μm. Capacitances of the gate-source and gate-drain electrodes are different by choosing the upper (lower) electrode as a source (drain). Furthermore, the capacitance between the top electrode and gate electrode is controllable by changing the gate width. Typical capacitances of gate - lower electrode and gate - upper electrode were 0.3 and 2.3 pF, respectively (gate electrode width; 8 μm).

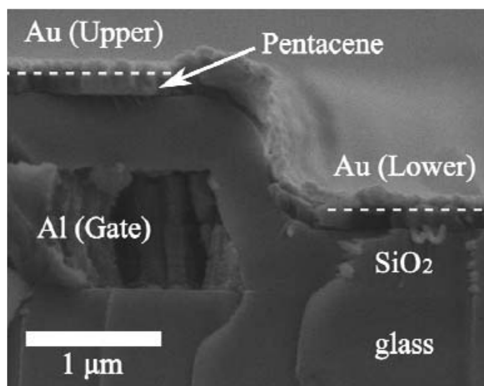


Fig. 2. SEM micrograph around the step-edge region of SVC-OFET.

3. Results and discussion

The static characteristics of the pentacene SVC-OFET are shown in Fig. 3 (a) and (b). The drain-source current (I_{DS}) at constant drain-source voltage (V_{DS}) decreases with increasing the gate voltage (V_G). These characteristics are same as a typical p-channel pentacene OFET. The mobility and ON/OFF ratio were approximately 0.05 cm²/Vs and 10^3, respectively. However, FET characteristics connecting to the lower electrode as a source (Fig. 3 (a)) show no current saturation in the measurement region. The difference of FET characteristics is mainly due to the asymmetric structure of SVC-OFET such as the formation of accumulation layer, contact resistance, etc.

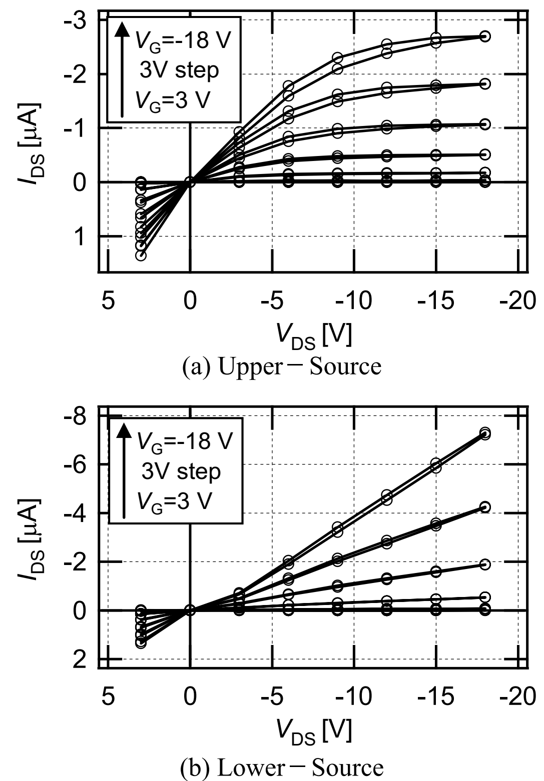
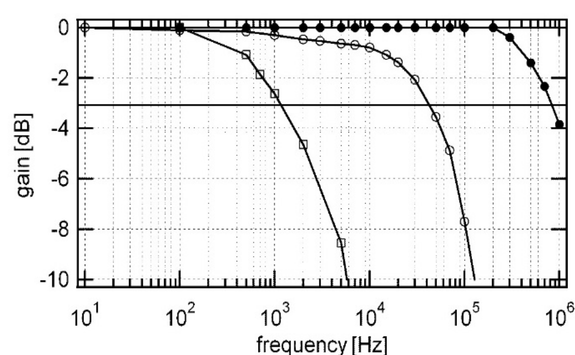


Fig. 3. Static characteristics of the pentacene SVC-OFET.

Figure 4 shows frequency characteristics of SVC-OFETs. As a reference, the experimental data of a pentacene lateral-type FET with the channel length of 20 μm are shown in Fig. 4. X-axial shows frequency of gate voltage and Y-axial shows the gain which is the ratio of the output Ids at each frequency (Ids(f)) to that at 10 Hz (Ids (10 Hz)). The cut-off frequency (fc) is defined here as the frequency where Ids(f) decreases to 3 dB down value from the Ids(10Hz) ; $20\log(I_{DS}(f_C)/I_{DS}(10Hz)=-3$ [dB]). As shown in Fig. 4, fc was approximately 50 kHz for upper-source. On the other hand, fc was 7 kHz for lower-source (the data are not shown in Fig. 4). These results indicate that the capacitance between the gate and upper electrode influences the frequency characteristics.

The control of pentacene crystal size and alignment is effective to improve the mobility of pentacene film and frequency characteristics. We applied self-assembled monolayer of 1,1,1,3,3,3-hexamethyldisilazan（HMDS）[8] between pentacene and SiO_2 layer. The HMDS surface modification improves fc toward higher frequency around 800 kHz as shown in Fig. 4. The fc obtained here is very high value comparing

other type of OFETs.



□: Lateral-type OFET, fc = 1.2 kHz
○: No HMDS treatment SVC-OFET, fc=50 kHz
●: HMDS treatment SVC-OFET, fc=800 kHz

Fig. 4. Frequency characteristic of SVC-OFET and lateral-type OFET.

4. Summary

New type OFETs with short channel length (SVC-OFETs) have been fabricated and investigated the basic characteristics. SVC-OFETs showed excellent device performances and high cut-off frequency approximately 800 kHz was obtained. These results demonstrate that SVC-OFETs have a potential to produce an active matrix display elements with a simple fabrication process.

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6. References

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