5-3: *[Invited]* Roll-to-Roll Manufacturing of Electronics on Flexible Substrates Using Self-Aligned Imprint Lithography (SAIL)

Han-Jun Kim*, Marcia Almanza-Workman, Alison Chaiken, Richard Elder, Bob Garcia, Warren Jackson, Albert Jeans, Ohseung Kwon, Hao Luo, Ping Mei, Craig Perlov, Carl Taussig
Hewlett Packard Labs, Palo Alto, CA, USA

Frank Jeffrey, Kelly Beacom, Steve Braymen, Jason Hauschildt, Don Larson
PowerFilm Inc., Ames, IA, USA

Phone: (650) 857-8525, E-mail: han-jun.kim@hp.com*

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Abstract

We are working towards large-area arrays of thin film transistors on polymer substrates using roll-to-roll (R2R) processes exclusively. Self-aligned imprint lithography (SAIL) is an enabler to pattern and align submicron features on meter-scaled flexible substrates in the R2R environment. The progress, current status and remaining issues of this new fabrication technology are presented.

1. Introduction

Low-cost manufacturing of display electronics on flexible substrates has seen a great amount of interest and endeavors recently. Flexible substrates undergo nonuniform deformations during device fabrication, so the conventional photolithographic tools requiring precise layer-to-layer alignment are difficult and costly to implement.

Self-aligned imprint lithography (SAIL) solves the challenge of patterning and aligning submicron features on meter-scale substrates by encoding the geometry for all of the patterning steps into discrete heights of a monolithic three dimensional masking structure, which maintains alignment regardless of process induced substrate distortion. The fact that geometrical encoding of multiple layer information reduces the entire patterning process to a mere single embossing step is also advantageous since in a conventional flat panel process the materials and processing costs are dominated by the multiple applications of photoresist and the subsequent exposure, development, and stripping of that material. As a result, film deposition, patterning, and etching steps are separated into different process modules, thereby more easily run under steady state conditions. In such ways, the SAIL process is highly compatible with roll-to-roll (R2R) processing. Defect control and yield consideration have become the major challenges as we move from basic feasibility demonstrations to full R2R fabrication.

This paper discusses the progress we have made in our processes and tools, along with our first demonstration of E-Ink based electrophoretic displays which use SAIL active matrix backplanes fabricated directly onto flexible substrates.

2. SAIL TFT devices

All the TFT materials are deposited in the same chamber without breaking the vacuum. Continuous deposition of the full TFT stack avoids contamination and reduces the footprint of deposition equipment, minimizing the clean room requirements. The complete stack consists of an adhesion layer, gate metal, dielectric, hydrogenated amorphous Si, n+ microcrystalline Si, and top metal to the source and drain. The films are deposited sequentially onto the polymer substrate. The highest process temperature incorporated is 250 ºC.

In the SAIL process, all the geometric information needed to pattern each and every layer is contained in a monolithic, three-dimensional mask structure, which presents discrete modulations of step thickness. Since this pre-aligned masking structure distorts with the substrate whenever a dimensional change occurs, critical interlayer alignments are preserved throughout the entire processing steps no matter how much the substrate deforms. Figure 1 illustrates this unique and important feature of the SAIL process, and compares

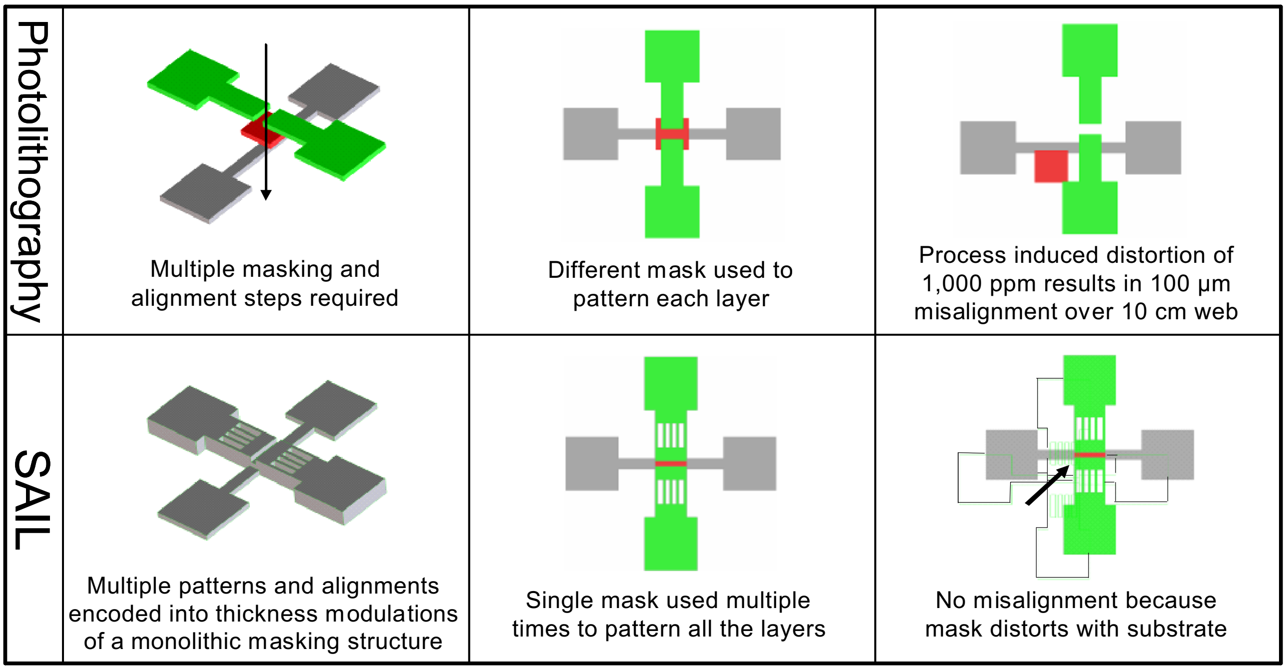

Figure 1. Schematic diagrams comparing photolithography and the SAIL process, where alignments are preserved throughout the entire processing steps because the masking structure distorts with the substrate

with the photolithographic process when a noticeable amount of substrate distortion is introduced.

Once a pre-aligned 3-D mask is imprinted on top of the TFT stack, a series of selective etches are applied to uniformly thin down the entire mask structure one level at a time, thereby patterning each stack layer, and eventually, fabricating the electronic devices.

Electrical transfer characteristic of an individual SAIL transistor is represented in Figure 2. In this graph, the source drain current divided by W/L, where W is the channel width and L is the channel length both in microns, are indicated in the legend. The on current for the channels, where L=1 •m, is about 90 •A, the on/off ratio is 10^7, and the mobility is 0.34 cm^2/Vs. The source/gate and drain/gate overlaps are about 2 •m, resulting in low overlap capacitance. The current scales with 1/L, indicating the contacts are able to deliver high current densities. The SAIL transistor performance is sufficiently high to be suitable for producing backplanes for LCD and even OLED displays. Addressable active matrix arrays have been fabricated and tested. Currently, arrays which have up to 24 x 38 pixels and areas around 10 cm^2 have been produced and demonstrated with E-Ink electrophoretic capsules as the front plane. These arrays have been produced in our research laboratory without the use of a clean room.

3. Flexible, R2R SAIL technology development

The objective of the SAIL process development is to push towards full scale commercialization of end-to-end R2R manufacturing process on flexible substrates. A brief summary of the approach taken towards such commercialization consists of roughly four different phases.

In the first phase, the focus was primarily on individual component technology development. First of all, the stack films were deposited onto flexible substrates to optimize basic material properties. The Many years of experience and expertise Powerfilm Inc. had developed for photovoltaics facilitated R2R deposition. The dielectric was optimized for breakdown strength, leakage, and ability to withstand mechanical flexing. The doped Si contacts were optimized for thickness and ability to deliver high on currents. Stresses in all the layers were investigated and minimized. SAIL masks were hand imprinted, and devices were patterned using standard batch process, targeting individual TFTs rather than arrays. R2R imprinting and dry etching systems were designed and built. Handling and testing procedures for flexible substrates were developed.

In the second phase, individual technological components were combined, and various design rules

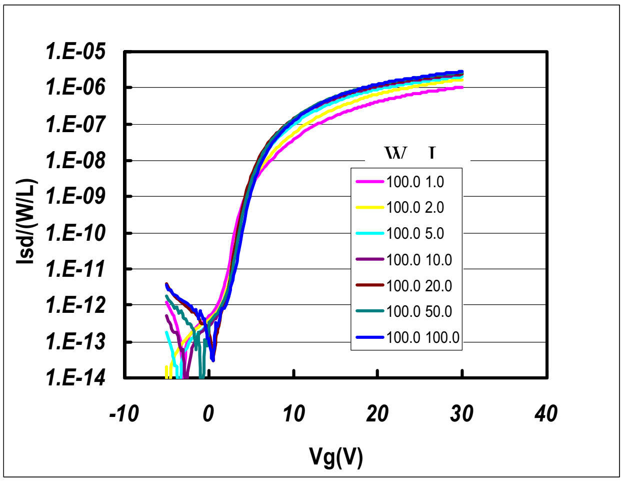

Figure 2. Source-drain current, I_{sd}, divided by W/L versus gate voltage, V_g, for SAIL transistors on 50 µm thick polyimide substrate (as a function of channel width, W, and length, L)

for imprint lithographic structures and masks were developed. Devices were produced using R2R SAIL embossing on flexible substrates, but etching was still performed in the standard batch mode. Stamp wear and lifetimes were evaluated and improved. The devices on the roll were subjected to mechanical flexure tests. Few if any of the transistors failed as a result of the mechanical stressing. The metal lines appear to be the most sensitive to repetitive mechanical flexing, a problem faced by all flexible electronic technologies. The resulting TFT arrays serve as display backplanes, which are bonded to various front-planes such as E-Ink electrophoretic capsules. Figure 3 shows our first demonstration of E-Ink based flexible display that is driven by a 38 x 24 pixel SAIL active matrix backplane.

In the third phase, which is currently near the completion, devices and arrays are being produced using full R2R SAIL process on flexible substrates, from deposition to patterning, and to wet and dry etching. So far, the process has been scaled up to 13" width, and the fabrication processes developed in the prior phases are transitioned to the newly built equipments dedicated for the R2R imprinting and etching. Figure 4 shows active matrix backplanes being fabricated on a continuous 13" wide roll. All the steps of film deposition and patterning, along with most of dry and wet etching steps are being performed in the R2R environment. Procedures for identifying the major sources of array defects have been implemented, and fixtures for rapidly testing full arrays are operational. Optical inspection for the imprinting, etching, and defect yield counting steps are being implemented. Rather simple changes as reduction in particulates from the deposition systems, improved cleaning procedures, and improved process monitoring are making large reductions in defect rates which are already on the order of 0.1 defects per cm^2.

In the final phase, the focus will move to yield improvement so that the commercial viability of SAIL can be validated. To achieve this goal, defect analysis, real time process monitoring, and design rule modification are being undertaken in order to produce full display sized arrays with a high yield. Finally, methods for integration with the front-planes, contacting the flexible electronics, passivation, and packaging are needed.

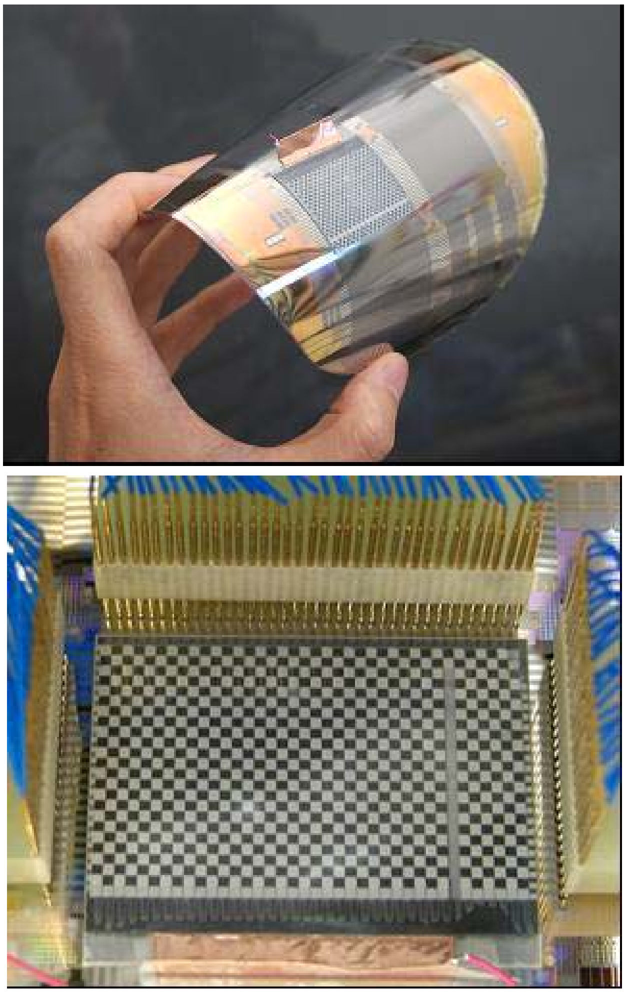

Figure 3. First E-Ink-based SAIL flexible display driven by a 38 x 24 pixel active matrix backplane built on PEN substrate

Figure 4. Active matrix backplanes fabricated on continuous 13" wide web. All the steps of film deposition and patterning, along with most of dry and wet etching steps were performed in the R2R environment.

Once the yield reaches an acceptable level, more efforts will be made to improve the overall throughput and speed of any rate limiting process, thereby further enhancing the cost effectiveness of the process.

4. Summary

We have developed the SAIL process which enables precision patterning and interlayer alignment on dimensionally unstable flexible substrates. High performance transistors and addressable active matrix arrays have been fabricated and tested. Integrating the SAIL backplanes with E-Ink front planes has led our first demonstration of fully R2R compatible SAIL prototype displays. Improvements we have made in our tools and processes were also discussed. Defects and yield are among the major concerns as we move from basic feasibility demonstrations to full R2R fabrication of electronic devices. The SAIL process is not only enabling a technology but also capable of significantly reducing the cost of manufacturing.

5. Acknowledgements

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6. References

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