a- Si:H TFT Level Shifter with Reduced Number of Power

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Abstract

We proposed a-Si:H TFT (hydrogenated amorphous silicon thin film transistor) level shifter which reduced number of power sources. To reduce the number of power sources from four to two, modified bootstrapped inverter was used for the level shifter. The shift register was verified by PSPICE circuit simulation and fabricated. The fabricated level shifter successfully shifted low input (0 to 5 V) to high level output (-7 to 23 V).

1. INTRODUCTION

Hydrogenated amorphous-silicon thin-film transistors (a-Si:H TFT's) are well known as switches associated with pixel elements in active matrix liquid-crystal displays (AMLCD's). Their characteristics are a rather low field effect mobility (0.5 cm^2/V-sec), a low leakage current in the off state (below 0.1 pA), and uniform TFT parameters over very large substrate. In spite of low field effect mobility, a-Si:H TFT can also be used to build row drivers of the AMLCD directly on glass with simple circuit schematics [1] [2] .

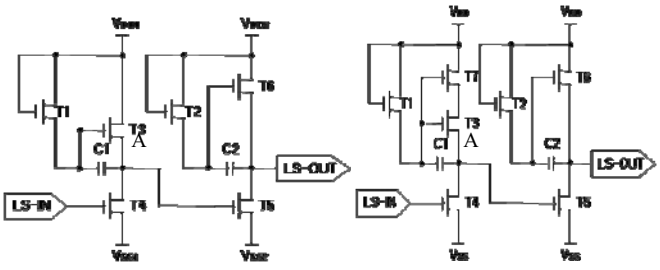
The integrated circuit using a-Si:H TFT has several advantages. First, most of the TFT-LCD manufacturers are based on a-Si:H TFT technology. Second, a-Si:H TFT process is suitable for large area applicati ons because of its low cost, low temperature processing and better uniformity over large area substrates. Third, the module cost can be reduced by eliminating the drive IC's and related processes.

Drive voltages of a-Si:H TFT gate driver are higher than those of conventional logic devices. Therefore, additional chips for level shift are being used. However, we had proposed integrated a-Si:H TFT level shifter which operated well with 5 V input signals.

Another a-Si:H TFT level shifter was proposed to reduce power consumption [3]. The drawback of both level shifters is to use four power sources; V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2}. To reduce the number of power sources, a new a-Si:H TFT level shifter is proposed [4].

2. PROPOSED a-Si:H TFT LEVEL SHIFTER

Fig. 1 (a) shows previous level shifter which used four power sources (V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2}). The new proposed level shifter is shown in Fig. 1 (b). Proposed level shifter uses only two power sources; V_{DD} and V_{SS}..

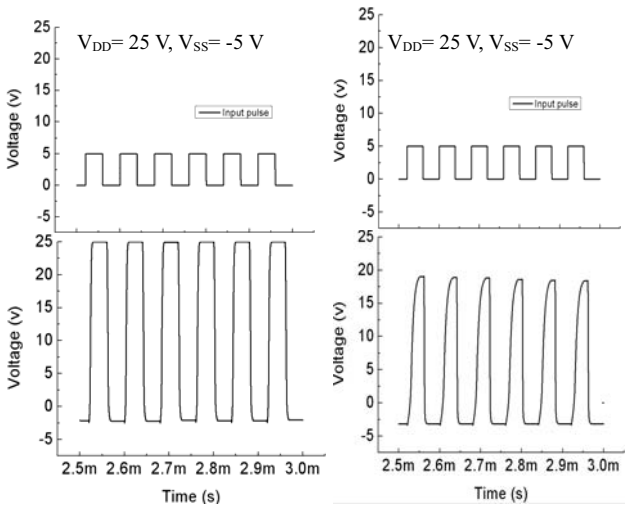


(a) (b)

Fig. 1 (a) Schematic of previous a-Si:H TFT level shifter, (b) proposed a-Si:H TFT level shifter.

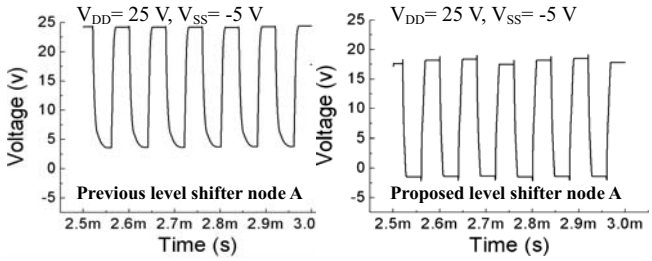
The proposed circuit used bootstrapped inverter. Previous level shifter used 6 TFTs and 2 capacitors but, proposed level shifter uses 7 TFTs and 2 capacitors. The previous level shifter used four power sources. However, proposed level shifter used only two power sources.

Fig. 2 (a) shows output of previous level shifter for V_{DD1}=15 V, V_{DD2}=25 V, V_{SS1}=-7 V, V_{SS2}=-9 V and Fig. 2 (b) shows output of previous level shifter for V_{DD1}= V_{DD2}=25 V, V_{SS1}=V_{SS2}=-5 V.



(a) (b)

Fig. 2 (a) output of previous level shifter for V_{DD1}=15 V, V_{DD2}=25 V, V_{SS1}=-7 V, V_{SS2}=-9 V, (b) output of previous level shifter for V_{DD1}= V_{DD2}=25 V, V_{SS1}=V_{SS2}=-5 V.



(a) (b)

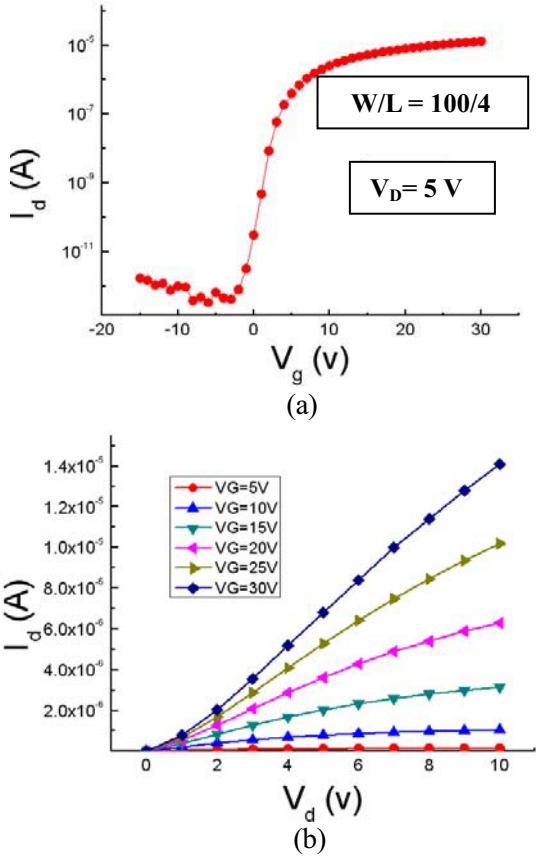
Fig. 3 (a) Node A output of previous level shifter, (b) node A output of proposed level shifter.

Previous level shifter shows deformed output waveform for common V_{DD} and V_{SS}. However, proposed a-Si:H TFT level shifter shows better waveform. The level shifter is composed of two cascaded inverters. The output of the first inverter is the input of the second inverter. We compared the output of the first inverter for both the previous and proposed level shifter.

Figure 3 (a) shows the output of the first inverter of the previous level shifter and Fig. 3(b) shows for the proposed one. The output of the previous one shows long fall time compared the proposed one. The output of the proposed one shows shorter fall time and shifted to the lower voltage.

3. FABRICATION

The proposed a-Si:H level shifter was designed and fabricated with a a-Si:H TFT process. Fig.4 shows transfer curve of fabricated a-Si:H TFT (a) and output curve (b). The channel length (L) and width (W) of this TFT are 4 μm and 100 μm, respectively.



(a)

(b)

Fig.4 (a) Transfer curve of fabricated a-Si:H TFT, (b) output curve of fabricated a-Si:H TFT.

Figure 5 shows optical image of fabricated proposed level shifter. Input of proposed level shifter was 0-5 V and measured output was -7 ~23V.

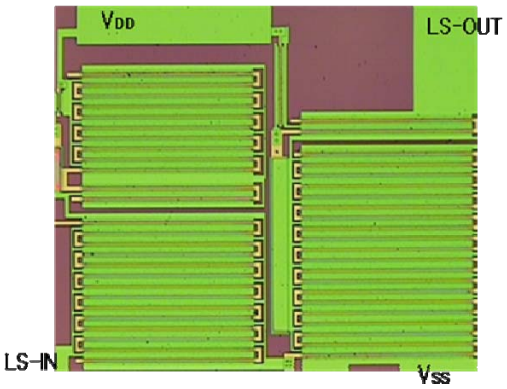


Fig. 5 Optical image of fabricated proposed level shifter.

Input of proposed level shifter is 0 ~ 5 V and output is -7 ~ 23 V. This output pulse can be used for a-Si:H TFT shift register.

4. RESULTS AND DISCUSSION

We fabricated level shifter of common power voltage. With 0 ~ 5 V input square wave into the level shifter, we got a level shifted square wave. We measured the output of the fabricated level shifter for the input square wave of 0 ~ 5V.

Figure 6 shows input and output of the proposed level shifter. V_{DD} and V_{SS} were 30 V and -10 V, respectively. The input square wave was 2 kHz. The output-high voltage and output-low voltage were 23 V and -7 V, respectively. The rise and fall times were 15 μs and 8 μs, respectively.

Fig. 6 shows input and output of proposed level shifter.

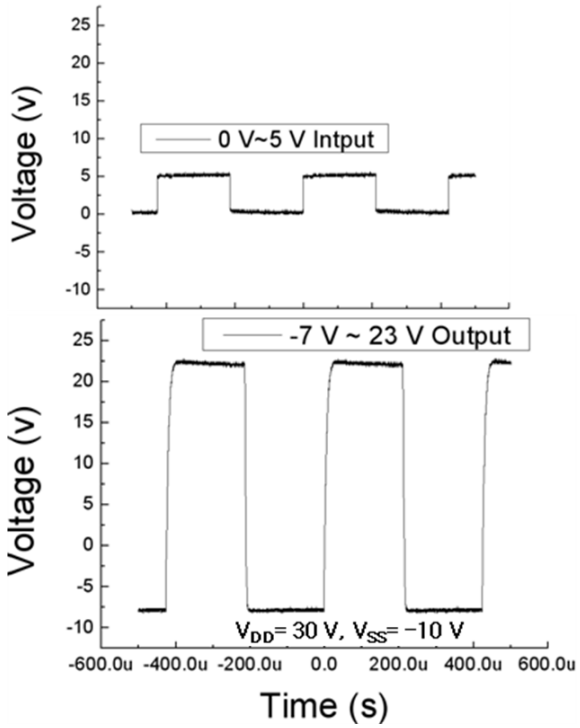
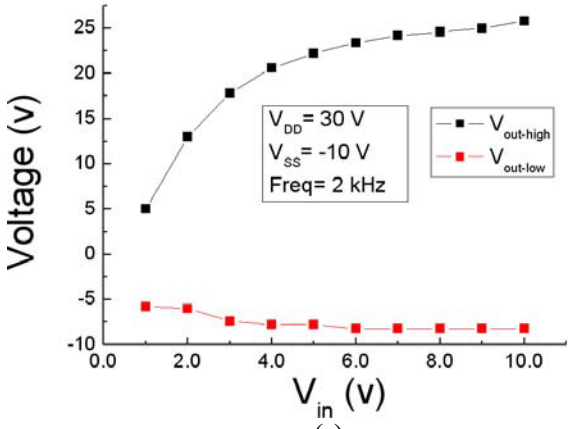
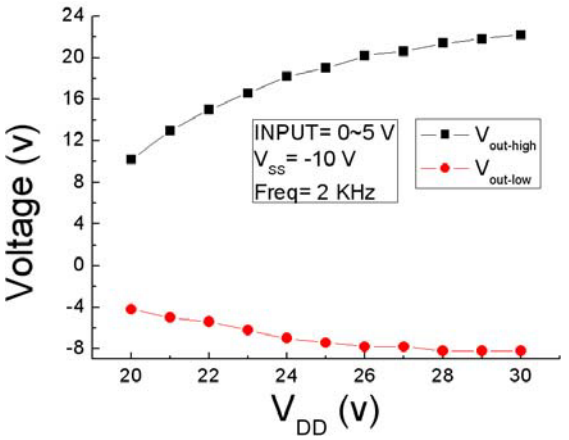


Fig.6 Input and output of proposed level shifter.

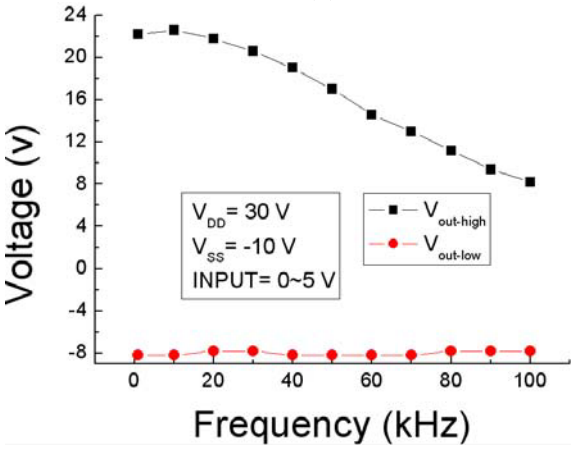
We measured the characteristics of fabricated level shifter.



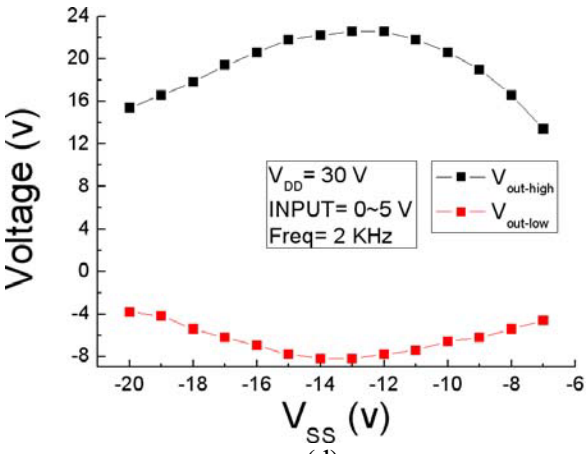
(a)



(b)



(c)



(d)

Fig. 7 (a) $V_{out\text{-}high}$'s and $V_{out\text{-}low}$'s for various input voltages, (b) for various Vdd's, (c) for various frequencies of input square wave.

Fig. 7 (a) shows the voltages of $V_{out\text{-}high}$ and $V_{out\text{-}low}$ for various input voltage. The output shows best characteristic to 0 ~ 10 V voltage level. Fig. 7 (b) shows the voltages of $V_{out\text{-}high}$ and $V_{out\text{-}low}$ for various V_{DD}'s. Fig. 7 (c) shows the voltages of $V_{out\text{-}high}$ and $V_{out\text{-}low}$ for various input square

wave frequencies. Fig. 7 (d) shows the voltages of $V_{out\text{-}high}$ and $V_{out\text{-}low}$ for various V_{SS}'s.

Output high level depends on power voltages, V_{DD} and V_{SS}. We can optimize each values for the required output high and low voltages.

5. Summary

We proposed a-Si:H TFT level shifter which reduced the number of powers from four to two. The fabricated proposed a-Si:H TFT level shifter shifted input(0 to 5 V) to the output of -7 to 23 V, successfully. The output level depends on V_{DD}'s, V_{SS}'s and input level. The level shifter gave -7 to 23 V output for single V_{DD} and V_{SS} which is advantage of the proposed one compared to the previous one which used four powers.

We will be the level shifter embedded shift resister and the proposed level shifter measured stability.

6. References

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