Views on the low-resistant bus materials and their process architecture for the large-sized & post-ultra definition TFT-LCD

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Abstract

For the large-sized and post-ultra definition TFT-LCD, improved drivability is prerequisite not only for the integration of driving circuit on glass but also for the chargeability of each pixel. In order to meet required drivability, currently adopted process architecture and materials are modified for the RC delay reduction, including the drastic increase of gate bus thickness and its related solution for step coverage. We present new process architecture and material selection for the next generation TFT-LCD devices.

1. Introduction

TFT-LCD seems to sweep over the whole FPD market with versatile products and high displaying quality. Many new technologies have been suggested to improve its device performance and manufacturing productivity. In terms of efficient productivity and device performance, less-mask process based on slit-photolithography made it possible to achieve 4 mask process as general manufacturing method and C/F on array also realized in the maximum aperture ratio of the pixel by fully self-align between TFT array and C/F layer, respectively [1-3].

But, to get more aggressive expansion of TV and DID market, some breakthroughs are still needed to meet the driving scheme and panel brightness. In the application of large-sized and high-resolution devices, the distortion of gate signal due to the RC (resistance-capacitance) delay are supposed to aggravate insufficient charging of TFT array and lack of driving marginality, which is more critical to the devices with high refresh rate of more than 120 Hz preventing motion blur effect [4]. Up to now, Cu has been known as the best way to overcome RC delay of gate signal for large-sized and high-resolution TFT-LCD due to its low resistivity, resulting in Cu-based process architecture for manufacturing method. But, its effect on RC Delay reduction by low resistivity was limited and proved to be insufficient in many application because currently adopted Cu process are designed with very thin Cu film less than 0.4 μm [5].

In this paper, we reviewed noble process architecture for RC delay reduction featuring with formation of thick Cu gate and its related process, which meets the required driving scheme of large-sized and post-ultra definition TFT-LCD.

2. Experimental

In TFT-LCD, RC delays for the gate and data signal are inherently unavoidable by the resistance of bus-line itself and parasitic capacitances between overlapped layers. As the panel size and its resolution increase, the distortion of gate signal is more aggravated and detrimental to the insufficient charging of TFT arrays. Considering driving scheme and aspect ratio of the TFT-LCD panel, reduction of gate RC delay is more important than data's. In order to reduce gate RC delay, the reduction of gate-bus resistance is preferred than that of parasitic capacitance. Considering the width of gate bus is limited by aperture ratio, the formation of thick gate bus with low resistivity is the most effective solution in terms of material selection and process architecture, which still remains the disadvantages of step coverage caused by thick gate. Finally, breakthrough point of process architecture for RC delay reduction is comprised of the formation of thick Cu gate to reduce the resistance of gate bus-line and its planarization for subsequent staggered structure. In this paper, detailed noble process architectures were evaluated in different ways, electro-less plating of thick Cu with trench process and patterning of sputtered-thick Cu with subsequent planarization process, which meets the

required driving scheme of large-sized and post-ultra definition TFT-LCD.

3. Results and discussion

Although thick Cu process by electro-plating method has been generally used in damascene process during wafer fabrication, it took disadvantages in TFT-LCD fabrication due to thickness non-uniformity over the large glass substrate [6]. Figure 1 shows process flow for ELP (electro-less plating) process for thick Cu gate formation.

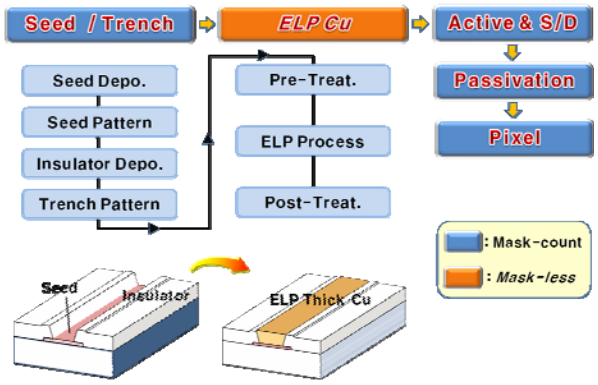


Fig.1. Process flow for ELP Cu process

After patterning of seed metal layer, trench-well was formed by the deposition of inorganic transparent insulator and photolithography-based dry etching.

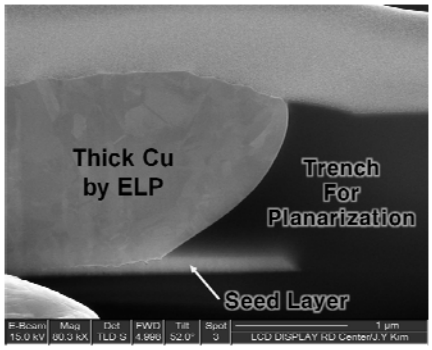


Fig.2. Thick Cu gate by ELP & trench

The electro-less plating process of thick Cu can be divided into 3 partial steps. Surface treatment of seed layer was done by plasma-assisted or solution-based cleaning before the main ELP process, we manipulated ELP process to achieve uniform growth of thick Cu film by controlling the chemical contents of solution, process temperature, and process time, etc. Finally, post-heat treatment for Cu bus line in inert ambient was done to decrease the resistance and increase the adhesion to seed layer. Although ELP process took advantage in stress release for thick film growth, resistivity of the thick Cu could not meet its bulk value due to the impurity injected during solution process and ELP solution itself, moreover, singular behavior of Cu growth and interaction with trench-well caused high surface roughness and poor flatness as figure 2 shows, resulting in step coverage demerits for subsequent thin films process and staggered structure.

Currently, thin Cu-based 4 mask process, patterning of sputtered-thin Cu with wet etching method, are adopted for LCD panel production and estimated as highly competitive manufacturing method, showing many advantages in terms of process simplification and quality enhancement. Although the simplest way of RC delay reduction is to increase the thickness of gate bus, several conditions are required to guarantee the process reliability such as stress release induced by thick Cu deposition and process capability by solution-based etching.

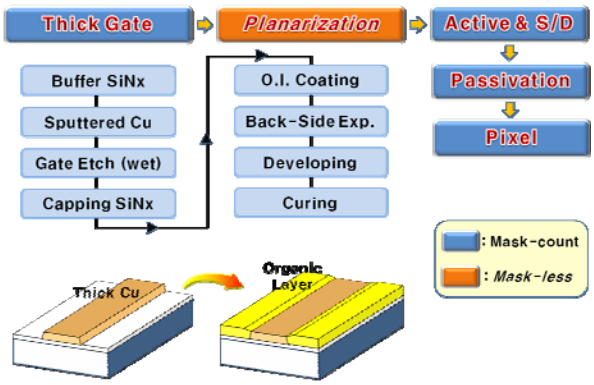


Fig.3. Process flow for Sputtered Cu process

Tensile stress acting on the interface between sputtered Cu and glass substrate are supposed to increase whereas the resistance of Cu gate is decreased by increasing the Cu thickness. Therefore, SiNx-based buffer layer, inducing compressive stress, was pre-deposited to relieve the stress between thick Cu and glass substrate. Optimized stress control between Cu and buffer SiNx made it possible to deposit thick Cu up to 2.0 μm without causing potential problems for glass bending through the whole process. Elaborated mixture of wet etchant was developed to pattern thick Cu gate with enhanced etch

rate and desired high taper angle for subsequent planarization process by back-side exposure. Finally, capping SiNx layer was deposited to prevent Cu and its surface from contaminating by any organic and acidic source.

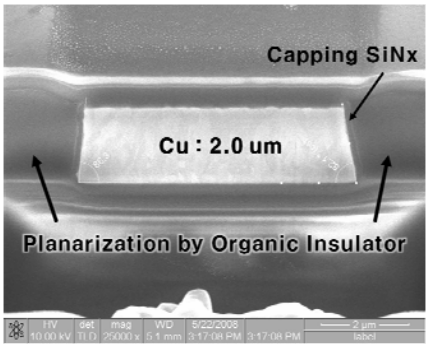


Fig.4. Thick Cu gate by sputter & planarization

In order to fabricate inverted staggered TFT structure after gate process, planarization of patterned thick Cu gate was needed to avoid possible step coverage demerits. To fill-out the empty space between thick Cu gates, negative photo-sensitive organic insulator was coated over the whole glass substrate and back-side exposure was applied. Back-side exposure method with organic insulator has merits in our proposed RC delay reduction process, which benefits low production cost by mask-less process without expensive photolithography equipment, and exact patterning by virtually self-aligned method. Key factor for planarization process by back-side exposure were taper angle of thick gate and material properties of organic insulator, such as reflow marginality at designed curing temperature and transmittance after heat treatment.

After evaluating both proposed structures, in terms of quality enhancement, process simplification, cost saving effect, eco-friendly process, compatibility with current process, and process reliability as a manufacturing method, sputtered-thick Cu gate with planarization process was proved to be better structure. In order to get desired RC delay reduction as expected by increasing Cu gate thickness, 4 mask process was applied to fabricate TFT arrays and pixels. Deposition of continuous three silicon-based layers, including SiNx:H, a-Si:H and n+a-Si:H, was followed by thin Cu data and its barrier layer. After typical procedure for slit-photolithography, such as 1st S/D patterning, active etch, PR etch back, 2nd S/D patterning and n+a-Si etching, was successively processed, whole TFT arrays and pixels were fabricated by passivation and pixel formation.

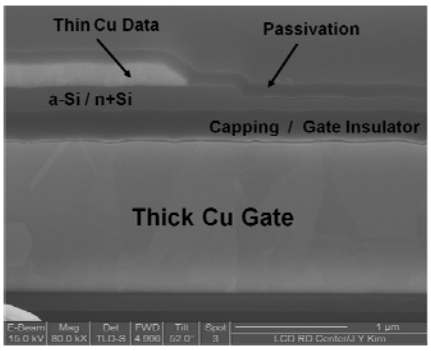
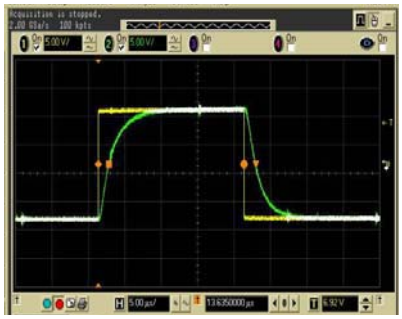


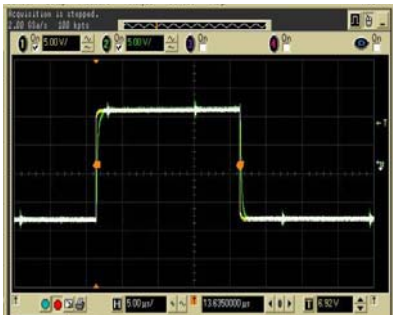
Fig.5. Cross-sectional view for TFT array

Back-side exposure for planarization of organic insulator made it possible to achieve RC delay reduction process architecture without additional mask and realize productivity-oriented mass production method.

We fabricated 30-inch full high definition compatible device with aforementioned RC delay reduction process by modifying the driving scheme of 15-inch XGA.



a.Thin Al 2500Å



b.Thick Cu 20000 Å

Fig.6. Comparison on RC delay reduction

Figure 6 shows RC delay comparison between typical thin Al gate of 2500Å and proposed thick Cu gate of 20000Å. RC delay of 4.23 μsec at the thin Al gate has reduced to 0.41 μsec by more than 90%, resulting in an idealistic shape of gate output signal from enormously distorted at the thin Al case. Although the difference in gate widths and wet-etch capability has to be considered into data analysis, it is clear that our proposed thick Cu gate and its related process are most effective method to improve drivability reduced by RC delay in TFT-LCD.

4. Summary

Next-generation flat panel displays are required to have not only low cost competitiveness but also technical breakthrough. In addition to brightness and color reproducibility, high refresh rate becomes more important factor deciding display quality, especially in the application of large-sized and high-resolution TFT-LCDs. In the near future, more than 70-inch sized QFHD (3840*2160) TFT-LCD with 240 Hz would replace 40-inch sized FHD (1920*1080) TFT-LCD with 120 Hz, which requires TFT-LCD's drivability to the extreme condition. In the case that currently adopted thin Al and Cu process could not meet the required driving scheme for next-generation display, proposed RC delay reduction structure with thick Cu gate and related process, integrated with high mobility switching materials, would be effective solution to the TFT-LCD makers.

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5. References

1. J.H. Song, S.G. Kim, H.W. Nam, S.G. Roh, J.H. Lee, D.S. Sakong, and J.H. Souk, SID Intl Symp Digest Tech Papers, 1018 (2000)
2. J.H. Song, D.J. Kwon, S.G. Kim, N.S. Roh, H.S. Park, Y.B. Park, D.G. Kim, C.O. Jeong, H.S. Kong, C.W. Kim, and K.H. Chung, SID Intl Symp Digest Tech Papers, 1038 (2002)
3. J.H. Song, S.G. Kim, H.S. Park, C.O. Jeong, C.W. Kim, and K.H. Chung, J. SID., 203 (2003) 11/1
4. Y. Yoshida, Y. Kikuchi, S. Daly, and M. Sugino, SID Intl Symp Digest Tech Papers, 1852 (2005)
5. Y.S. Hwang, G.C. Jo, G.S. Chae, and I.J. Chung, IDMC, 205 (2003)
6. K.N. Tu, J. Appl. Phys., 5451 (2003) 94/9