

Failure Mode Test and Analysis of Light Emitting Diodes (LEDs) for General Lighting Applications

N. Hwang, K.C. Lee, S.H. Park, Y.I. Cho, and Y.M. Yu

Korea Photonics Technology Institute, 971-35 Wolchul-dong Buk-gu, Gwangju 500-779, Korea

INTRODUCTION

Recent technology development of light emitting diodes (LEDs) is very much promising to be applied to many applications such as automotive, streetlights, big outdoor displays, and general lighting. The optical power and efficacy of LEDs are now compatible and superior to the conventional lighting systems. The degradation of lighting parameters by employing LEDs as lighting sources has become very important for various solid state lighting applications, where the high electrical power is required to produce enough brightness for general lighting purpose. Consequently, the inevitable high thermal energy dissipated from LED chips is considered to be the key degradation factor. The failure analysis of LEDs is a quite sophisticated procedure since the LED failure is a combinational mechanism from electrical over stress to thermal dissipation that is critical to sustain a good reliability performance since continuous operation at high temperatures degrades LED characteristics with decrease of light output as well as the color shift of light emission. The purpose of this paper is, then, to investigate the failure mechanism of LEDs through the predefined intentional failure mode simulation. Typical failure modes of general semiconductor devices in operational environments are highlighted by the specific test conditions such as excessive current or voltage in forward or reverse bias. By observing various individual failure patterns after applying failure mode simulation tests, the failure analysis of LEDs can become a failure matrix mosaicking with the identified failure patterns.

EXPERIMENT

The LEDs used in this study were packaged in a SMD PLCC type 3528 size including GaN/InGaN small size chips, by a domestic company. In this work, over 150 devices were studied. A semiconductor test and analyzer (ELECS EL-421C) was used to evaluate the operational electrical characteristics of LEDs.

A total of 4 test conditions were predetermined to identify the effect on the failure patterns by individual stress factors as follows:

1. Forward over-current @ $IF=100 \text{ mA} \rightarrow 200 \text{ mA} \rightarrow 300 \text{ mA}$ for 3 min. per level till to fail.
2. Reverse over-current @ $IR=1 \text{ mA} \rightarrow 5 \text{ mA} \rightarrow$

- 10 mA for 3 min. per level till to fail.
 3. HBM ESD stress @ 8 kV, 3 times, 1 sec.
 4. MM ESD stress @ 1 kV, 3 times, 1 sec.

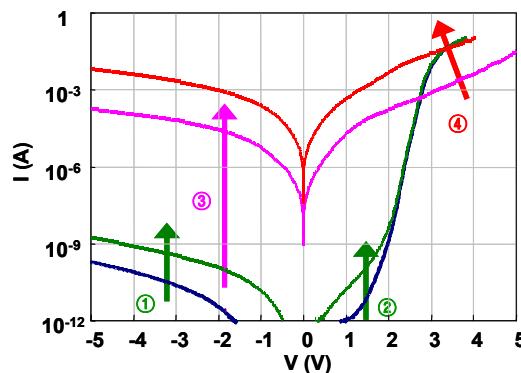


Fig. 1 Typical IV characteristics of LEDs before and after the forward over current test.

RESULTS & DISCUSSIONS

Case 1: Forward over current

Fig. 1 shows the typical IV characteristics of LEDs before and after the forward over current stress test. The failure procedure was monitored as follows:

- increase of the leakage current in the reverse region by a shunt component through the defects within pn junction,
- increase of the recombination-generation current at a low voltage region by depletion region effect,
- increase of the leakage current at full operational region by generation of defects within pn junction,

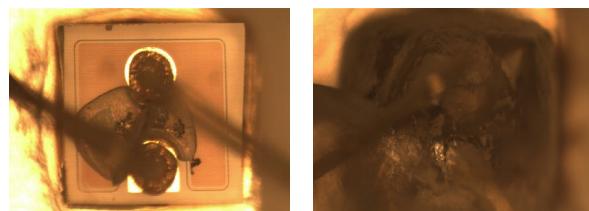


Fig. 2 Failure pattern of LEDs after the forward over current test.

Fig. 2 shows the failure patterns of LEDs after the forward over current stress test. The degenerated epoxy is found to be hard to remove under the normal depackaging process. Excessive thermal energy deformed the epoxy on the top surface between two electrodes.

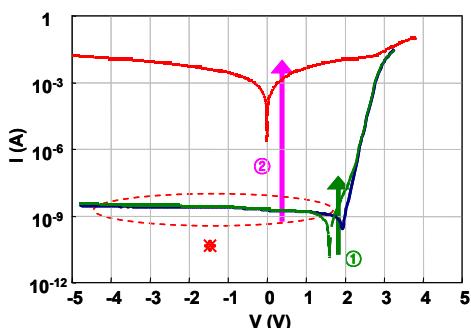


Fig. 3 Typical IV characteristics of LEDs before and after the reverse over current test.

Case 2: Reverse over current

Fig. 3 shows the typical IV characteristics of LEDs before and after the reverse over current test. The failure procedure was monitored as generation of diode parasitic effects with lower barrier height causing leakage current through a defective region within pn junction. ※ Photocurrent generation was found under room lighted conditions.



Fig. 4 Failure pattern of LEDs after the reverse over current test.

Fig. 4 shows the failure patterns of LEDs after the reverse over current stress test. The surface damage was found to be partitionable with a non-emitting region.

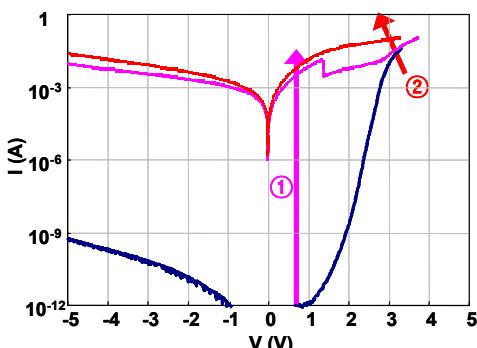


Fig. 5 Typical IV characteristics of LEDs before and after the HBM ESD stress test.

Case 3: HBM ESD Stress

Fig. 5 shows the typical IV characteristics of LEDs before and after the HBM ESD stress test. The failure procedure was monitored as same as the failure pattern of the reverse over current stress, the high voltage impact shock seems induced high surface charge current leaving point burnt marks.



Fig. 6 Failure pattern of LEDs after the HBM ESD stress test.

Fig. 6 shows the failure patterns of LEDs after the HBM ESD stress test. The severe burnt mark points were found as well as a non-emitting region.

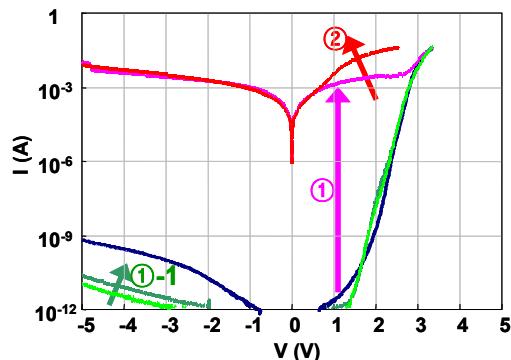


Fig. 7 Typical IV characteristics of LEDs before and after the MM ESD stress test.

Case 4: MM ESD Stress

Fig. 7 shows the typical IV characteristics of LEDs before and after the MM ESD stress test. The failure procedure was monitored as same as the failure pattern of the HBM ESD stress, the high current impact shock seems accumulated high thermal energy leaving epoxy degeneration around the electrode.



Fig. 8 Failure pattern of LEDs after the MM ESD stress test.

Fig. 8 shows the failure patterns of LEDs after the MM ESD stress test. The surface damage is much like the combination of forward and reverse over current failures.

CONCLUSION

In summary, failure analysis of LEDs has been studied under simulated failure tests. With the predesigned failure mode and its failure pattern, the investigation of failure mechanism is self-instructional by employing the results of failure mode simulation. The major failure mode of LEDs is found and confirmed to be related with internal thermal energy accumulation.