DC Bus Conditioner을 위한 가변히스테리시스제어

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A Variable Hysteresis Control for a DC Bus Conditioner

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Abstract - A DC distributed power system(DPS) has many loads with varied functions. In particular, there may be large pulsed loads with short duty ratio, which can affect the normal operation of other loads. In this paper, a bi-directional converter with inductive storage is used as a DC bus conditioner to damp voltage transients on the bus. In addition, the constant frequency hysteresis control technique for a DC bus conditioner is presented. A simple and fast prediction of the hysteresis band-width is implemented by the phase-lock loop control, keeping constant switching frequency. This technique offers the excellent dynamic response in load or parameter variation. The control performance is illustrated by simulated results with the SABER package. The proposed hysteresis control results in the shortest and the smallest excursions.

1. Introduction

"Distributed Power Systems" (DPSs) has been widely used various industrial/military applications such as spacecraft, aircraft, telecommunications, autonomous production lines, and defence electronic power systems. DPSs offer many advantages to power system designers: high power capability, high efficiency, reliability, modularity, redundancy, expandability, and reduced development cost [1-2].

In a high voltage DC distribution power system, DC bus instability due to system interaction is one of the greatest concerns. A DC DPS is made up of smaller power subsystems. Usually these smaller subsystems are designed individually, i.e. the design of each subsystem is only based on the stability requirement for its stand-alone operation. As a result, after system integration, the interaction between subsystems may cause performance degradation, and even system instability [3]. The resulting transients on the supplying voltage bus inevitably influence the rest of the loads and may affect their normal operation [4].

In a DC power distribution system, DC bus instability mainly may result from the negative impedance due to the constant power loads, pulsed loads, system transients and so on. Thus, a DC bus conditioner may be used to mitigate the voltage transients on the bus. "DC Bus Conditioners" are power electronic converters that dampen the voltage transients on the bus. They achieve this by transiently injecting current into the bus. These DC bus conditioners can be divided into two types: voltage-storage and current-storage. One of the drawbacks of the voltage-storage DC bus conditioner is that it inherently does not fully utilize the storage capacitor energy. The drawback of the current-storage DC bus conditioner is large power losses of the storage inductor, however this can be overcome with the use of cryogenic power electronics and superconducting coils. Therefore, the current storage DC bus conditioner will be an attractive solution for all future DC DPS.

The choice and implementation of the controller for a DC bus conditioner is very important for the achievement of a satisfactory performance level. Hysteresis control is one of many excellent controllers used widely in power electronic converter applications[5]. This control technique has the advantage of not only being simple, robust and stable regardless of load condition, but also having a very good transient response and inherent peak limiting. However, the main disadvantage is that the switching frequency varies significantly with line and load variation. This results in the load current harmonic ripple and irregular converter operation. Alternatively, an effective control technique to eliminate these inconveniences is hysteresis control with constant switching frequency (with variable hysteresis band) [6-7]. The implementation of adapting hysteresis with a constant switching frequency could be easily implemented by "Phase Lock Loop" (PLL). In this paper, a current-storage DC bus conditioner using constant frequency hysteresis control is used.

2. Converter Operation and Design

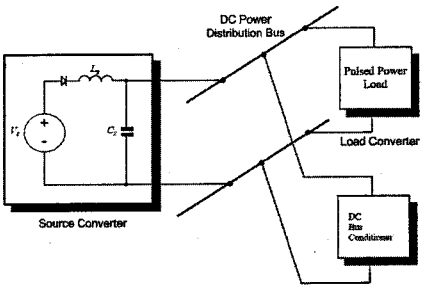

Fig 1. A simple DC distributed power system

Fig. 1 is a simple DC distributed power system configuration, which is used to investigate the operation and the performance of the bi-directional converter used as a DC bus conditioner. This DC DPS consists of three subsystems: 1) a source converter comprising a DC power source and a simple $L_S - C_S$ filter, 2) a pulsed power load, 3) a VBC. In this configuration, a VBC has been used to damp the DC bus voltage transients or instabilities.

The detailed schematic of the bi-directional converter with a storage

inductor, is shown in Fig. 2. It includes a filter capacitor C_F, a storage inductor L_{ST}, and four power switches $Q_1 \sim Q_4$. The current I_S is the source current including the disturbance current and the current I_C is the filter capacitor current. The voltage V_C is the DC bus voltage and the current I_{LST} is the storage inductor current. Also, the current γ is the transiently injected current into the DC bus from the storage inductor, in order to compensate for the finite impedance of the DC bus. Also, the injection current γ can be expressed as

$$\gamma = \begin{cases} +I_{LST} & \text{for } Q_1, Q_2 = on \\ -I_{LST} & \text{for } Q_3, Q_4 = on \end{cases} \quad (1)$$

In Fig. 2, it assumes that the storage inductor has a smooth DC current. The filter capacitor C_F is used to reduce switching current ripples, which are caused by the conduction of a diagonal pair of switches (Q_1, Q_2) or (Q_3, Q_4).

In Fig. 1 and 2, if the pulsed power load is activated, the filter capacitor current I_C will be negative, due to the drop of the DC bus voltage. The bi-directional converter will then recognize this change and adjust the duty ratio accordingly, to facilitate the net flow of current back to the DC bus from the storage inductor. That is to say, when switches (Q_3, Q_4) are turned on, the energy of the inductive storage decreases and the DC bus voltage increases. Conversely, if the pulsed power load is deactivated, the filter capacitor current I_C will be positive because of the rise of the DC bus voltage. In order to adjust to this new condition, the bi-directional converter acknowledges the rise in the DC bus voltage and draws current to charge up the inductive storage, storing the

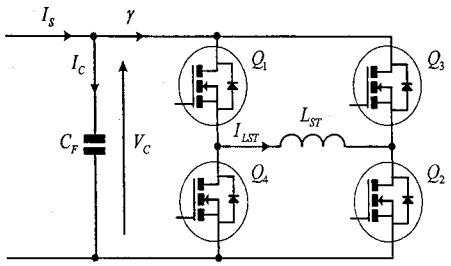

Fig. 2. A DC bus conditioner with inductive storage

excess energy to release when required. Namely, when switches (Q_1, Q_2) are turned on, the energy of the inductive storage is increases and then the DC bus voltage is decreases. Therefore, the converter regulates the energy flow through the storage inductor by means of the proper switching action, and the switching action is dependant on the bus status. The energy stored in the inductor L_{ST} depends on the the square of the current flowing through it. Thus, the DC bus voltage may be stabilised through the DC bus conditioner with inductive storage.

In order to look into the dynamics of the converter and the performance of the controller, the typical system parameters have to be used. The DC input supply voltage V_S was chosen at 270 V. Also, a synchronous machine is generally used as a generator. This machine, directly coupled to the engine shaft, provides the excitation. The output voltage is controlled by modulating the excitation of the synchronous machine, which is a fairly slow process, usually with a bandwidth of less than 10 Hz. The 400 Hz three-phase output of the generator is rectified with a full wave rectifier followed by a second-order input filter. Thus, the corner frequency of around 1 kHz for this filter was chosen, providing ample attenuation of the low-frequency ripple of the rectifier. The input filter components L_S =400 μH and C_S=50 μF was chosen. There are two important characteristics of this arrangement. Firstly, the rectifier blocks reverse current flow into the generator. Secondly, the impedance and the corner frequency of the input filter dominate the transients on the DC bus.

In this study, a step-up (boost) converter is used as a short pulsed load. The step-up converter appears as a constant power load because it is tightly regulated. A short pulsed power load separately draw 20 A from the DC bus in the steady state. These loads are activated and deactivated at 90 Hz with a 50% duty ratio.

Furthermore, in our particular application, a short pulsed power load is rated at 10 J. Thus, the energy storage capability of the inductor is also 10 J. The average current of the load is 20 A, resulting in value of the inductor L_{ST} =50 mH. The switching frequency of the DC bus conditioner was chosen to be 100 kHz, well within the capabilities of all power MOSFETs. The value of 10 μF for the filter capacitor C_F is calculated, to limit the resulting voltage ripple to around 1 % nominal voltage, i.e. 2.7 V.

3. Constant Frequency Hysteresis Control

In Fig. 3, the hysteresis control (in effect a type of SMC) has implemented attempts to respond instantaneously to voltage variations while keeping the switching frequency within the prescribed limit. Only the inductor charge and discharge modes are utilised. The switch states are determined by a comparator, which keeps the AC component of the bus voltage within the limits $v_{ac}^* \pm (\beta/2)$, β being the hysteresis bandwidth and v_{ac}^* being the desired bus voltage variation, δ is a instantaneous bus voltage error $(v_{ac} - v_{ac}^*)$.

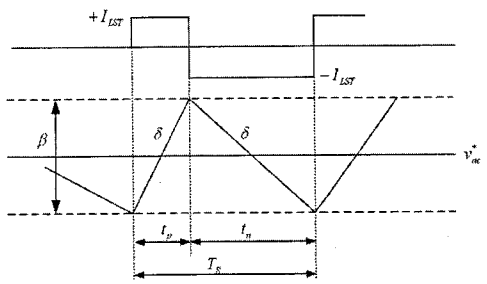

Fig. 3. Simplified waveforms for hysteresis control

In Fig. 2 and Fig. 3, the filter capacitor current I_C can be written as follows

$$I_C = C_F \frac{dV_C}{dt} \quad (2)$$

$$\therefore I_C = I_S - I_{LST} = C_F \frac{\Delta V_C}{\Delta t} = C_F \frac{v_{ac}}{\Delta t} \quad (2a)$$

For Mode 1, where the converter draws current from the bus, the switching time t_p is

$$I_S - I_{LST} = C_F \frac{\beta}{t_p} \quad (3)$$

$$\therefore t_p = \frac{\beta C_F}{I_{LST}(1 - I_n)} \quad (3a)$$

where $I_n = I_S / I_{LST}$.

Similarly, for Mode 2 and converter sinking current from the bus, the switching time t_n is

$$I_S + I_{LST} = C_F \frac{\beta}{t_n} \quad (4)$$

$$\therefore t_n = \frac{\beta C_F}{I_{LST}(1+I_n)} \quad (4a)$$

Thus, the switching period can be then calculated as

$$T_S = \frac{1}{f_s} = t_p + t_n = \frac{2\beta C_F}{I_{LST}(1-I_n^2)} \quad (5)$$

In equation (5), if I_n varies and β is constant, a variable switching frequency is produced. However, if the hysteresis band β varies in dependence of I_n, a constant switching frequency can be obtained from equation (5). Namely, the modulation law for the PLL (Phase-Locked Loop) keeping the switching frequency constant can be derived from equation (5).

$$\beta = \frac{I_{LST}}{2f_s^* C_F}(1-I_n^2)$$

$$\text{or } f_s^* = \frac{I_{LST}}{2\beta f_s^* C_F}(1-I_n^2) \quad (6)$$

where f_s^* is the desired switching frequency.

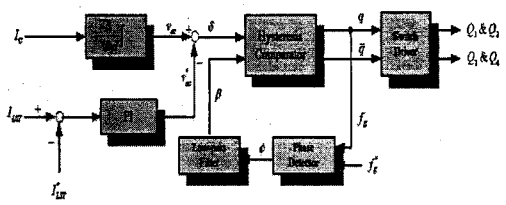

Fig. 4. Implementation of constant frequency hysteresis control

The implementation of the proposed controller is shown in the block diagram in Fig. 4. The hysteresis controller will keep the AC component of the bus voltage v_{ac} down to zero (as much as the storage current I_{LST} allows this) and will vary the hysteresis bandwidth in response to bus disturbances in order to limit the ensuing switching frequency variations. A phase detector compares the actual and the desired switching frequency. The output of the detector is filtered to produce a smooth value for the hysteresis bandwidth. A first-order filter was chosen for the purpose, with a corner frequency a decade below the targeted 100 kHz switching frequency. This somewhat conservative choice can be explained by the need for smooth signal for β.

4. Stability for the Proposed Hysteresis Controller

In Fig. 4, the transfer function of the first order filter is described with

$$TF\phi = \frac{d\beta}{d\phi} = \frac{k_f}{(s/\omega_c)+1} = \frac{k_f \omega_c}{s+\omega_c} \quad (7)$$

where k_f is a constant and w_c is a corner frequency of the filter.

The transfer function of the implemented phase detector can be approximated with

$$TF_{PHD} = \frac{d\psi}{df_s} = -\frac{2\pi}{s} \quad (8)$$

The hysteresis comparator is assumed not to introduce any dynamics or delays. From equations (5) and (6), its transfer function can be described as a DC gain only

$$TF_{HYS} = \frac{df_s}{d\beta} = -\frac{I_{LST}}{2\beta^2 C}(1-I_n^2) \quad (9)$$

By making use of equations from (5) to (9), the loop transfer function for frequency control is then

$$TF_{CLF} = \frac{4\pi C_F}{I_{LST}} \frac{f_s^{*2}}{(1-I_n^2)} \frac{k_f \omega_c}{s^2+\omega_c s} \quad (10)$$

$$= 2\pi \frac{k_f \omega_c}{s^2+\omega_c s} \frac{f_s^*}{\beta} \quad (10a)$$

In equation (10), the loop TF_{CLF} gain varies considerably with I_n. When I_n is very large, loop gain value approaches unity. On the contrary, for small value of I_n near zero the loop gain decreases. The loop gain TF_{CLF} of the equation (10a), also, varies appreciably with the hysteresis bandwidth β. Thus, the large variations of TF_{CLF} gain due to β or I_n may result in instability. To avoid instability, it is necessary to set the condition of I_n and the limit of the bandwidth β. From equation (6), the extremum values for β needed to keep the frequency constant can be calculated. For desired switching frequency and nominal storage current

$$\beta_{\min} < \beta < \beta_{\max} \quad (11)$$
$$\Rightarrow 0 < \beta < 10 \quad \text{for } 0 < I_S < I_{LST}$$

where f_s^*=100 kHz, C_F = 50 μF, and $0 < I_S < 20$.

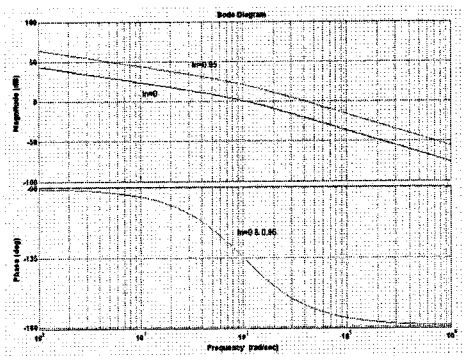

Fig. 5. Bode diagram of equation (10)

In Fig. 5, the asymptotic bode diagram for maximum and minimum diagram, corresponding to the choice adopted for the controller, are shown. The used parameters were: ω_c=10 kHz, f_s^*=100 kHz, I_{LST} = 20 A, I_{nmin}=0, I_{nmax}=0.95, $k = 0.2$, $L_{ST} = 50$ mH, and C_F = 50 μF,. Therefore, the transfer function in equation (10) resulta in a phase margin of 43 degree for $I_n = 0$ and 15 degree for $I_n = 0.95$.

5. PI Controller for Inductor Current Control

A second loop is needed to keep the storage current I_{LST} close to the desired level of 20 A ($I_{LST}^* = 20$ A). The reference input v_{ac}^* to the hysteresis comparator is modified by the error signal between the desired and the actual storage current. A proportional-integral compensator was used in this loop.

$$v_{ac}^{*} = k_p (I_{LST} - I_{LST}^{*}) + k_i \int (I_{LST} - I_{LST}^{*}) dt \quad (12)$$

From equation (11), the maximum value of β is 10. This means that the maximum current deviation is around 5 A. Since our target error is approximately 2A (10% of steady-state), the resulting proportionate gain should be 2. The required integral gain is to minimise any steady-state errors and compensate for the conduction losses in the power circuit. It therefore needs to be very low and in our simulation was set at 0.001.

6. Simulation results

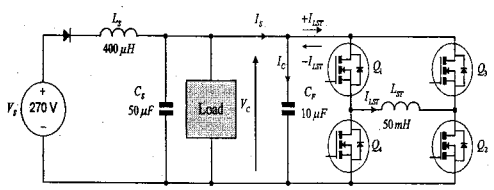

Fig. 6 The Proposed DC Bus Conditioner

To investigate the behaviour of the proposed controllers in a DC distributed power system with a DC bus conditioner, the worst-case scenarios are simulated here. A step-up (boost) converter is used as a short pulsed load. This is drawn 20 A from the DC bus in the steady state and are also activated and deactivated at 90 Hz with a 50% duty ratio. This means the case when the bus is transiently

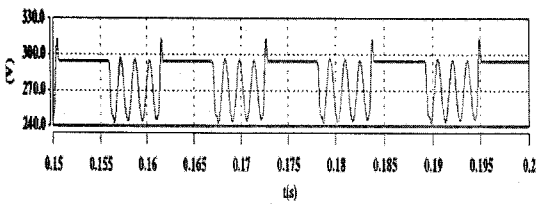

Fig 7. Simulation Results for a DPS without a DC bus condtiioner

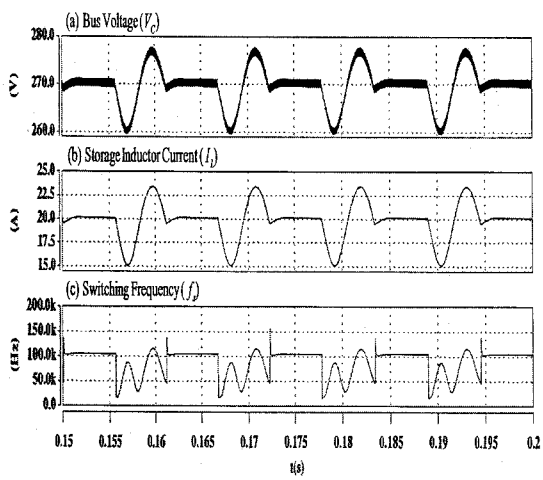

Fig 8. Simulation Results for a DPS with a DC bus conditioner

loaded from 0 % to 100 %.

The simulation results when the step-up converter is connected as a pulsed power load are shown in Fig. 7. In Fig. 7, the voltage variations on the bus voltage without DC bus conditioner are between 241 V and 315 V. When the load is activated, the large oscillations of 600 Hz, due to the interaction between the input filter and the filter of the boost converter, can also be seen. Also, as the load is deactivated, the peak voltage (315 V) is monitored and the voltage (315 V), higher than the nominal voltage (270 V), is observed.

As a result, the severe transients on the voltage bus, which are caused by short pulsed loads, result in a distributed power system. In fact, the resulting transients will heavily affect the normal operation of other loads and may result in instability in a DPS.

The simulation results for constant frequency hysteresis control are shown in Fig. 8. In Fig. 8(a), the bus voltage variations are certainly smaller than those of sliding mode control. The large excursions between 260 V to 276 V occur at load turn-on, as the available storage current cannot fully compensate for the larger disturbance current. For the duration of this instant, the DC bus conditioner sources the maximum available current to the bus and the switch configuration remains unchanged. This is demonstrated by a zero switching frequency (Fig. 8(c)). At load turn-off, the bus voltage recovers slowly toward its steady-state bus voltage. The average storage inductor current (Fig. 8(b)) is slightly higher than 20 A, experiencing transitions of +3/-4 A. The average commutation frequency is 98 kHz (Fig. 8(c), momentarily reaching 150 kHz during load turn on. This is well within the capabilities of advanced low on-state resistance MOSFETs.

7. Conclusion

The voltage bus conditioner (VBC) with inductive storage, as described in this paper, utilises all of the stored energy, unlike its counterpart with capacitive storage. The constant frequency hysteresis control resulted in the best performance. The bus voltage excusions are very well damped. The resulting transients at load turn-on are slightly, but noticeably smaller. Therefore, the proposed constant frequency hysteresis control results in the shortest and the smallest variations.

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