매트릭스 컨버터를 위한 새로운 예측 전류제어 펄폭 변조 방법

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Novel Predictive Current Control Pulse Width Modulation Method for Matrix Converters

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Abstract - A new pulse width modulation method based on predictive current control strategy is proposed to modulate matrix converters. The predictive current controller utilizes a discrete-time model to predict the future values of output currents and generates proper duty-ratios to minimize the output current errors. The proposed method uses continuous carrier and establishes a predictive current controller to predetermine duty ratio signal for directly generating gating signals an thus is named "predictive current control PWM(PCCPWM)".

The modulation algorithm and the required equations are derived by using average concept over one switching perio d. Thus it can be easily extended to other matrix converter topologies, especially with neutral connections, such as sing le-phase and two-phase matrix converters. The feasibility an d validity of the proposed strategy are verified by computer simulation and experimental results.

1. Introduction

Direct AC-AC converters based on matrix converter topology have been the researching interesting in recent years. Matrix converter contains an array of controlled semiconductor switches. These switches are forced on or off to generate desired output voltages with controllable input power factor [1]. Three major modulationtechniques are developed to control the three-phase to three-phase matrix converters; Alesina-Venturini method [2], space vector pulse width modulation(PWM) [3] and carrier based PWM [4]. However, Alesina-Venturini method and space vector PWM are not easy to implement because of requirement of complex calculation or lookup table initialization. The carrier based PWM in [4] implies relatively indirect understanding of matrix converter modulation because it involves discontinuous carrier waveform.

A "direct duty ratio PWM (DDPWM)" method for matrix converters, which is a carrier based PWM with continuous triangular carrier waveform is proposed in [5]. The proposed method generates proper duty-ratios to directly control a three-phase matrix converter. It can be easily implemented without complex calculation and lookup table. Based on the DDPWM method, this paper presents a novel PCCPWM method to modulate matrix converters. A discrete time model has been established to predict the future behavior of the converter system. Duty-ratios are properly generated in order to minimize the differences between load currents and their references. Input power factor are controlled by changing the slope of the carrier. The PCPWM does not require complex calculation and lookup table. The feasibility and validity of the proposed method have been verified by computer simulation and experimental results.

2. Proposed PCCPWM Controller

2.1 Proposed PCCPWM controller

Fig. 1 shows the circuit configuration including the three-phase input voltages, input filter, three-phase to three-phase matrix converter and resister-inductor(R-L) load.

If the only maximum one of the three line-to-line voltages is used as the input voltage to synthesize the output voltages during each switching period, then two of the three input phase voltages will be used. Consequently, one of the input phases does not conduct any current during the switching period, so that the input current will be distorted. The DDPWM uses two out of three of the line-to-line input voltages to synthesize the output voltages. Hence, all three input phases are utilized to conduct current during each switching period and, consequently, the input currents will not be distorted.

A switching period T_s can be divided into two sub-intervals, T_1 and T_2. Also, the maximum, medium and minimum input voltage values are designated as *MX*, *MD* and *MN* respectively.

During T_1, the line-to-line voltage between *MX* and *MN*, which is the maximum line-to-line voltage among the three line-to-line input voltages at the sampling instant, is used. During T_2, the second maximum line-to-line voltage, which is the larger one in *MX* to *MD* and *MD* to *MN*, is used. If *MX-MD>MD-MN*, *MX* to *MD* is used in T_2 and the switching pattern is named as switching pattern-I. Otherwise, if *MD* to *MN* is used in T_2, it is named as switching pattern-II.

Switching pattern-I: Fig. 2 shows the case of switching pattern-I for generating the *A*-phase output voltage, where the triangular carrier is compared with the duty ratio value, d_{A1}, resulting in the change of the output phase voltage such that *MN*→*MX*→*MD*.

Fig. 2 shows the actual *A*-phase output voltage synthesis when applying switching pattern-I. As seen in Fig. 2, *MN*, *MX*, *MX* and *MD* appear at the *A*-phase output terminal during T_{A1}, T_{A2}, T_{A3} and T_{A4} respectively. These four sub-intervals can be expressed as

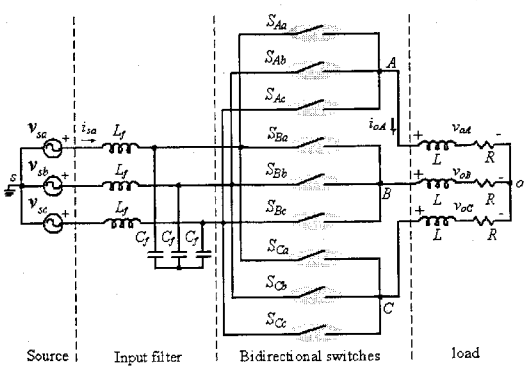

Fig. 1 Three-phase to three-phase matrix converter circuit

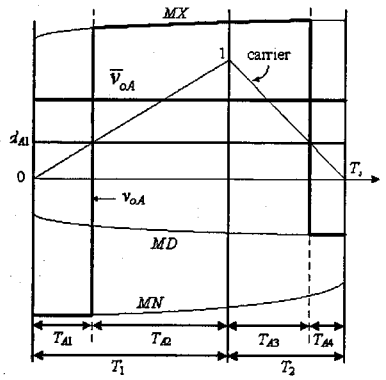

Fig. 2 Output *A*-phase voltage synthesis in switching pattern-I.

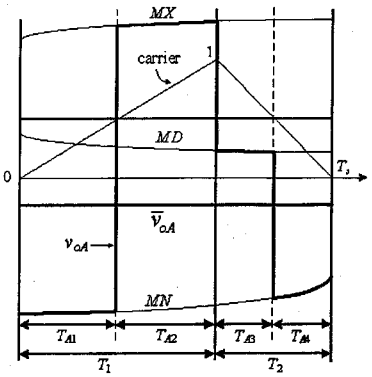

Fig. 3 Output *A*-phase voltage synthesis in switching pattern-II.

$$\begin{aligned} T_{A1} &= d_{A1} n T_s \\ T_{A2} &= (1-d_{A1}) n T_s \\ T_{A3} &= (1-d_{A1})(1-n) T_s \\ T_{A4} &= d_{A1}(1-n) T_s \end{aligned} \tag{1}$$

where d_{A1} is the *A*-phase duty ratio value when switching pattern-I is applied and n is defined as $n = T_1/T_s$ which involves the slope of the carrier.

Supposing that the input voltages are almost constant during the switching cycles, the integration of the output voltage v_{oA} over T_s can be written as

$$\int_0^{T_s} v_{oA}\, dt \cong T_{A1} \cdot MN + (T_{A2} + T_{A3}) \cdot MX + T_{A4} \cdot MD \tag{2}$$

Then, it is found from (1) and (2) that the averaged value of v_{oA} , $\overline{v}_{oA}$, can be approximated by

$$\begin{aligned} \overline{v}_{oA} &= \frac{1}{T_s}\int_0^{T_s} v_{oA} dt \\ &\cong d_{A1}(n \cdot MN - n \cdot MD + MD - MX) + MX \end{aligned} \tag{3}$$

In load side, the load current dynamics can be described by the equation

$$L \cdot \frac{di_{oA}(t)}{dt} + i_{oA}(t) \cdot R = \overline{v}_{oA} \tag{4}$$

A discrete-time model of (4) for a sampling time T_s can be used to predict the future value of load current. Fig. 4 shows the discrete timing sequence.

Approximating the derivative $di_{oA}(t)/dt$ by

$$\frac{di_{oA}(t)}{dt} \approx \frac{i_{oA}(k+1) - i_{oA}(k)}{T_s} \tag{5}$$

Replacing (5) in (4), the following expression is obtained for the future load current.

$$i_{oA}(k+1) = \frac{T_s}{L}\overline{v}_{oA}(k) - i_{oA}(k)\left(\frac{T_s R}{L} - 1\right) \tag{6}$$

Substituting (2) into (5) and solving for $d_{A1}(k)$,

$$d_{A1}(k) = \frac{(L/T_s) i_{oA}(k+1) - MX + i_{oA}(k)(R - L/T_s)}{n \cdot MN - n \cdot MD + MD - MX} \tag{7}$$

Forcing the predicted future load current value $i_{oA}(k+1)$ being equal to the future load current command $i_{cA}^*(k+1)$, then

$$d_{A1}(k) = \frac{(L/T_s) i_{cA}^*(k+1) - MX + i_{oA}(k)(R - L/T_s)}{n \cdot MN - n \cdot MD + MD - MX} \tag{8}$$

In (8), R, L and T_s are all known system parameters, MX and $i_{oA}(k)$ can be obtained by voltage and current sensing. Hence, if the future load current command $i_{cA}^*(k+1)$ is properly Determined, $d_{A1}(k)$ can be calculated.

The future load current command $i_{cA}^*(k+1)$ can be predicted from the present and previous values of the current reference. For sufficiently small sampling times T_s, it can be just assumed that $i_{cA}^*(k+1) = i_{cA}^*(k)$ and no extrapolation is needed. This approximation is considered in this paper.

Finally, the kth duty ratio $d_{A1}(k)$ can be determined by the following equation.

$$d_{A1}(k) = \frac{(L/T_s) i_{cA}^*(k) - MX + i_{oA}(k)(R - L/T_s)}{n \cdot MN - n \cdot MD + MD - MX} \tag{9}$$

Switching pattern-II: In the same way, switching pattern-II can be analyzed. Fig. 3 shows the output A-phase voltage synthesis in switching pattern-II. The same procedure as in switching pattern-I can be performed to establish a discrete time model and predict the future load current value, then the duty ratio value, d_{A2}, can be obtained as follows

$$d_{A2}(k) = \frac{(L/T_s) i_{cA}^*(k) - (n \cdot MX - n \cdot MD + MD) + i_{oA}(k)(R - L/T_s)}{MN - n \cdot MX - MD + n \cdot MD} \tag{10}$$

The duty ratio control law of the *A*-phase output is defined by (9) and (10). The other two output phases can be treated in the same manner.

2.2 Input current synthesis

In the duty ratio laws in (9) and (10), there is another degree of freedom, that is n. n can be properly adjusted to synthesize the sinusoidal input current, while maintaining T_s at a constant value. Under the condition of unit power factor, it can be found that n is determined by

$$n = \begin{cases} -MN/MX & \text{pattern-I} \\ -MX/MN & \text{pattern-II} \end{cases} \tag{11}$$

3. Experiment

To verify the feasibility of the proposed DDPWM methods, an experimental setup was built and the DDPWM controller was implemented by using TMS320VC33 DSP from Texas Instruments and Altera CPLD of EP1K100QC208-1. The experimental conditions are given in Table 1. The experimental configuration is shown in Fig. 4.

As seen in Fig. 4, two out of three input line-to-line voltages v_{sab} and v_{sbc} are sensed in order to calculate three input phase voltages v_{sa}, v_{sb} and v_{sc}. Sampled values of v_{sa}, v_{sb} and v_{sc} are then used to needed calculation. Input phase locked loop (PLL) is also incorporated into DSP to obtain input voltage angle θ_i and to determine the proper switching pattern. Three input phase currents i_{sa}, i_{sb}, i_{sc} are sensed only for protection purpose. Three output phase currents i_{oA}, i_{oB} and i_{oC} are sensed for both control and protection purpose.

The steady state experimental waveforms are shown in Fig. 5, when I^*_c=7A and f_o=30Hz. Fig. 5 contains the steady state experimental waveforms of the output line-to-line voltage v_{oAB}, output current i_{oA}, output current command i^*_{cA}, input voltage v_{sa} and input current i_{sa}. In Fig. 5, i_{sa} shows a small phase difference with the leading power factor, because of the input filter. It can be confirmed that the proposed DDPWM method is able to effectively synthesize both the output voltage and input current while achieving unity input power factor.

Fig. 6 shows the dynamic waveforms when I^*_c abruptly changes from 4A to 7A. Fig. 6 contains the flag signal which indicates the changing instant, the output line-to-line voltage v_{oAB}, A-phase output current command i^*_{cA} and A-phase output current i_{oA}. Fig. 6 also shows the expanded waveforms of i^*_{cA} and A-phase output current i_{oA}, $i^*_{cA\_exp}$ and i_{oA_exp} at the changing instant. As seen in Fig. 6, it can be confirmed that the PCCPWM controller operates quite well and it implies fast dynamic response.

4. Conclusions

This paper presents a novel PCCPWM based on the use of a continuous carrier to modulate matrix converters. The experimental results show that both the output voltages and input currents can be effectively modulated. It can be concl uded that the proposed method offers a very simple and eff ective way to modulate matrix converters.

Table 1 Experimental parameters

Rated Input voltage $V_{s\text{-}RMS}$	220V
Input filter L_f, C_f	100μH, 60μF
R-L load	20Ω-50mH
Input frequency f_i	60Hz
Switching frequency f_s	5kHz

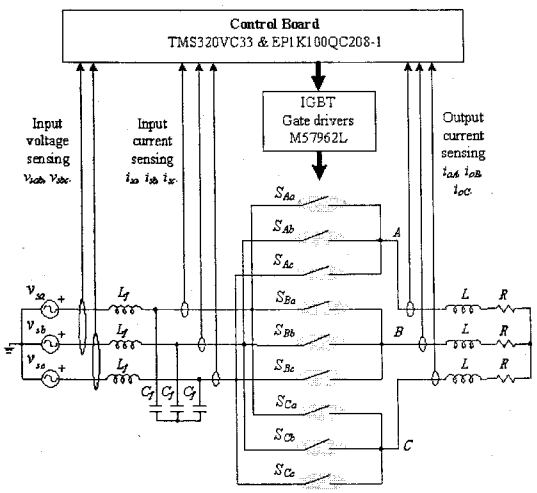

Fig. 4 Configuration of experimental setup

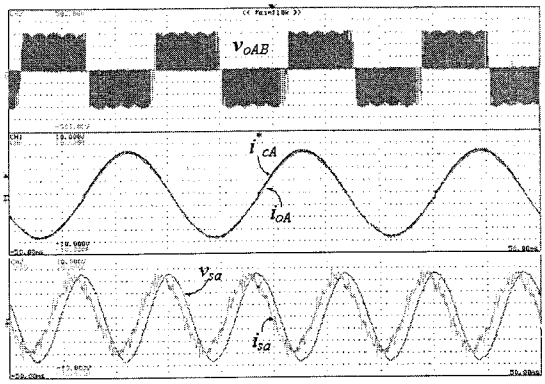

Fig. 5 Experimental waveforms: steady state operation v_{oAB} (100V/div, 10ms/div), i_{oA}(2A/div, 10ms/div), i^*_{cA}(2A/div, 10 ms/div), v_{sa}(50V/div, 10ms/div), i_{sa}(2A/div, 10ms/div).

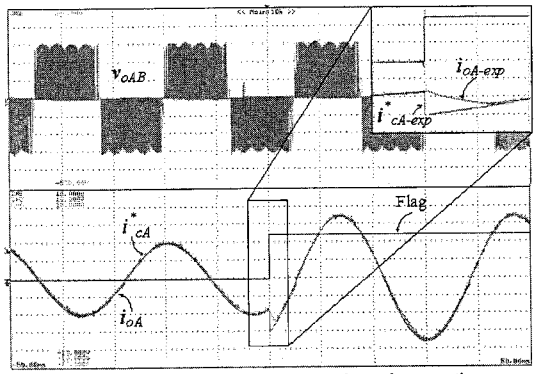

Fig. 6 Experimental waveforms: dynamic operation v_{oAB} (100V/div, 10ms/div), i_{oA}(2A/div, 10ms/div), i^*_{cA}(2A/div, 10 ms/div), v_{sa}(50V/div, 10ms/div).

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