A New Single-Stage PFC AC/DC Converter

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Abstract

A new ZVZCS Single-Stage Power-Factor-Correction(PFC) AC/DC converter with boost PFC cell is integrated with voltage doubler rectified asymmetrical half-bridge(VDRAHB) is proposed in this paper. The proposed converter features good power factor correction, low current harmonic distortions, tight output regulations and low voltage of link capacitor. An 85W prototype was implemented to show that it meets the harmonic requirements and standards satisfactorily with nearly unity power factor and high efficiency over universal input.

1. Introduction

Conventional off-line power converters with diode-capacitor rectifier front-end have distorted input current waveform with high harmonic contents. Since these converters have a low power factor, they cannot meet harmonic regulations and standards such as European line-current harmonic regulations defined in the IEC 61000-3-2 document and the Japanese input-harmonic current specifications. To comply with these standards, a number of single-stage and two-stage PFC circuits have been developed and reported in the literature. In the two-stage approach, it is customary to add a power-factor corrector ahead of the dc/dc converter to provide a regulated and isolated dc output. This approach has good characteristics of power-factor correction and fast output regulations, but the power-factor corrector increases the size and cost. Therefore, the two-stage approach is not desirable in low power applications [1].

Recently, many single-stage approaches have been suggested to achieve both power-factor correction and power conversion from the ac line to a desired dc output [2]. Since these topologies have a PFC cell is integrated with a DC/DC conversion cell and both cells share active switch and controller, single-stage approach is a better choice in cost point of view. Unfortunately, most of the proposed converters have one or more of the following disadvantages: large low-frequency output voltage ripple, low efficiency due to the switching loss and the rectification loss, variable switching frequency and high-voltage stress of switch. To overcome these disadvantages, the new single-stage PFC AC/DC converter with boost for PFC cell is integrated with VDRABH for DC/DC conversion cell is proposed. In this paper, to confirm the validity of the proposed converter, the operation principle and the experimental results of an 85W prototype will be presented.

2. Operational Principles

The circuit diagram of the proposed single-stage PFC AC/DC converter is shown in Fig. The proposed circuit is composed of a boost for PFC cell is integrated with a VDRABH for DC/DC conversion cell. The operation of the proposed converter can be classified into the three modes (t_0~t_2) and the corresponding

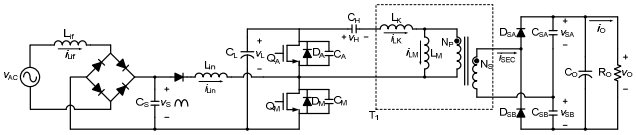

Fig. 1 Circuit Diagram of the proposed converter

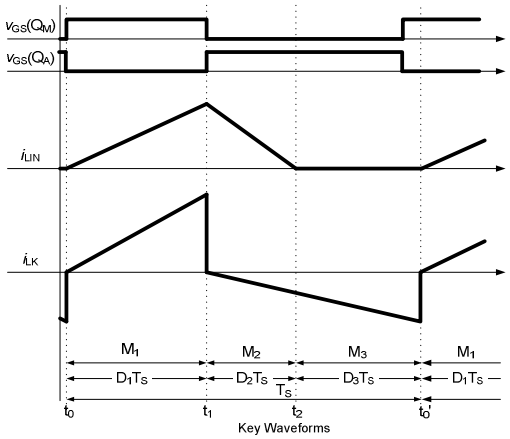

Fig. 2 Key waveforms of the proposed converter

waveforms are presented in Fig. 2.

Mode 1 begins at t_0 when Q_M is turned-on. The input voltage, v_S, is applied to the inductor L_{IN}, i_{LIN} starts to build up from zero. At the same time, (v_L-v_H) is applied to the primary winding of transformer T_1, i_{Lk} increases. Mode 2 begins at t_1 when Q_M is turned-off and Q_A is turned-on, respectively. (v_S-v_L) is applied to the inductor L_{IN}, i_{LIN} starts to flow through Q_A, and decreases to zero. -v_H is applied to the primary winding of T_1, i_{Lk} decreases. Mode 3 begins at t_2 when i_{LIN} decreased to zero and i_{Lk} decreases with same slope during mode 2. Mode 3 ends when Q_M is turned-on and starts another switching cycle at t_0`.

The voltage conversion ratio can be obtained, using the following equations.

$$D_1 = \sqrt{\frac{2\pi L_{IN} M_1 F_S}{R_{in}\int_0^{\pi} \frac{\sin^2\theta}{M_1 - \sin\theta}\, d\theta}}$$

where $M_1 = V_L / V_S$, $R_{in} = Ro / M_2^2$,

$$M_2 = \frac{V_O}{V_S} = \frac{\frac{N_S}{N_P} D_1^2 (1-D_1)^2}{D_1^2 (1-D_1)^2 + \frac{2L_k F_S}{R_O}\left(\frac{N_S}{N_P}\right)^2 \left[D_1^2 + (1-D_1)^2\right]}.$$

,where D_1 is duty ratio of Q_M and F_S is switching Frequency. DC conversion ratio of the M_1 and M_2 are plotted as a function of duty ratio in Fig. 3(a) and Fig. 3(b) with load variation, respectively, based on the design specifications and the circuit parameters for the 85W prototype in Table 1 and Table 2, respectively.

3. The characteristic of Link capacitor voltage

Conventional Single-Stage PFC AC/DC converter with PFC cell is operated in Discontinuous Conduction Mode (DCM) and DC/DC cell is operated in Continuous Conduction Mode (CCM) is shown in [4]. Since DC/DC cell is operated in CCM, duty ratio is not changed with load variation as shown in Fig. 3(c). Moreover, DC conversion ratio of the PFC cell increases according to decrease of load as shown in Fig. 3(a). Therefore, link capacitor voltage increases as load decreases. Since the high voltage stress and the impossibility of using commercial capacitor, increase of link capacitor voltage is one major problem of Single-Stage PFC AC/DC converter. In case of the proposed converter, however, the duty ratio is greatly changed with load variation as shown in Fig. 3(b). Although DC conversion ratio of PFC cell increases according to decrease of load like conventional Single-Stage PFC AC/DC converter, the duty ratio of the proposed converter largely reduced. Therefore, the increase of link capacitor voltage can be limited in spite of decrease in load. In case that DC/DC cell is operated in DCM, the increase of capacitor voltage also can be limited, since the duty ratio decrease as load decrease as shown in Fig. 3(d).

4. Experimental Results

To verify the operational principles and the feasibility of the proposed single-stage PFC AC/DC converter, the 85W prototype of the proposed converter has been implemented. The design specifications and circuit parameters of this prototype are same as presented in Table 1 and Table 2, respectively. Fig. 4 show the Boost PFC cell is operated in Boundary Conduction Mode(BCM) at 90 $V_{AC,RMS}$. The line input current follow the shape of the line input voltage as shown in Fig. 5 at 90 $V_{AC,RMS}$. The power factors and the efficiencies of the proposed converter are measured as presented in Fig. 6(a) and Fig. 6(b), respectively. The harmonic line currents of the proposed converter are analyzed as shown in Fig. 6(c). The proposed converter meets the harmonic requirements of IEC 61000-3-2 Standards. The voltage of link capacitor is sustained below 405V at line and load variations as shown in Fig. 6(d). Therefore, the commercial capacitor can be used in the proposed converter.

Table1. Design Specification

Specification	Value
Input voltage, V_S	90V ~ 270V_{AC_RMS}
Output voltage, V_O	18.5V
Max. output power, $P_{O,max}$	85W
Switching frequency, f_S	100kHz

Table2. Circuit Parameters

Parameter		Value
Transformer	N_P: N_S	F3805, 2EA, 1EA
	L_M	1.37mH
	L_K	12uH
C_H		2.2uF / 630V
C_{SA} & C_{SB}		22μF / 25V, 2EA

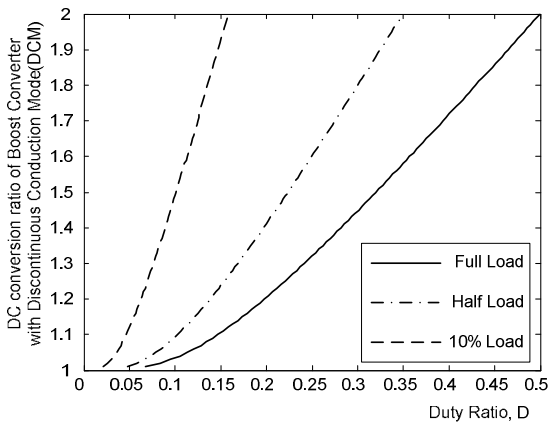

Fig. 3(a) DC conversion ratio of Boost with DCM

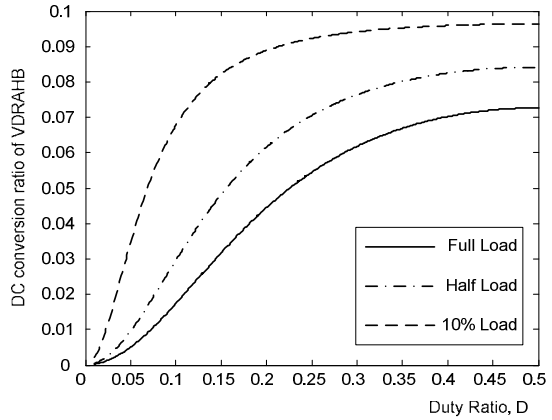

Fig. 3(b) DC conversion ratio of VDRAHB

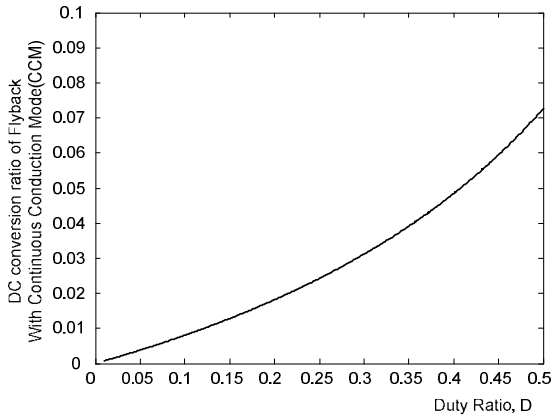

Fig. 3(c) DC conversion ratio of Flyback with CCM

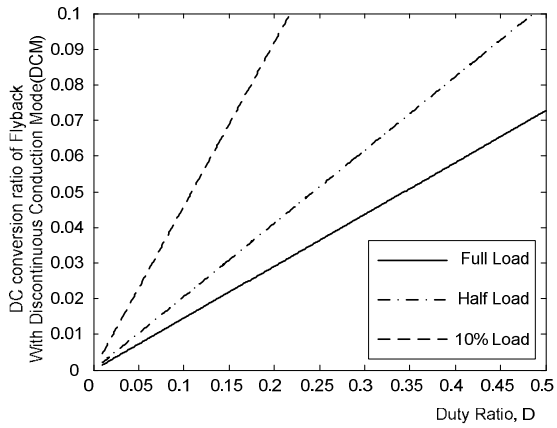

Fig. 3(d) DC conversion ratio of Flyback with DCM

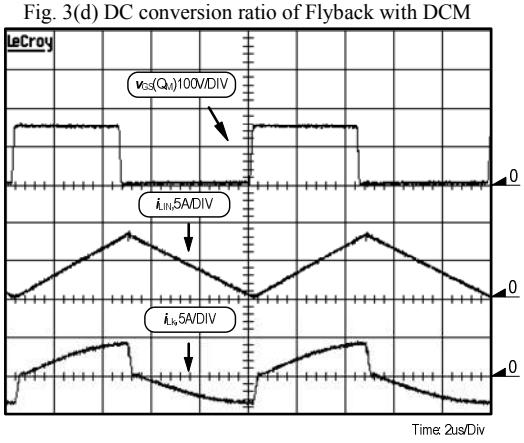

Fig. 4 Experimental Key waveforms

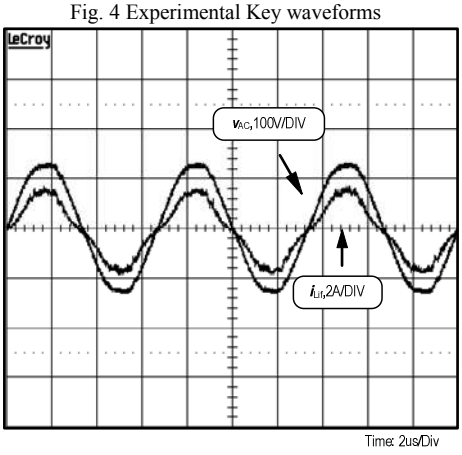

Fig. 5. Line Input Voltage and Current Waveforms

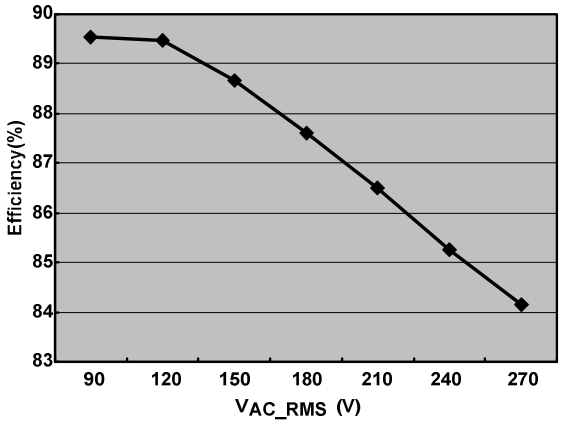

Fig. 6(a) Measured Efficiency

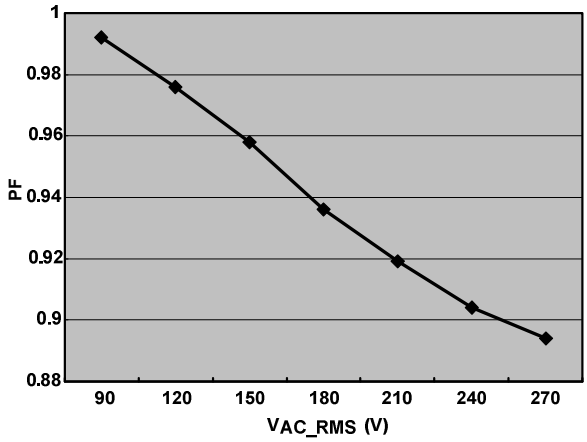

Fig. 6(b) Measured Power Factor

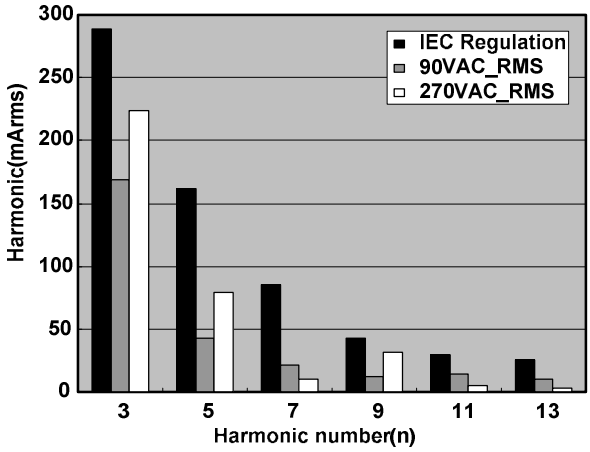

Fig. 6(c) Measured harmonic components

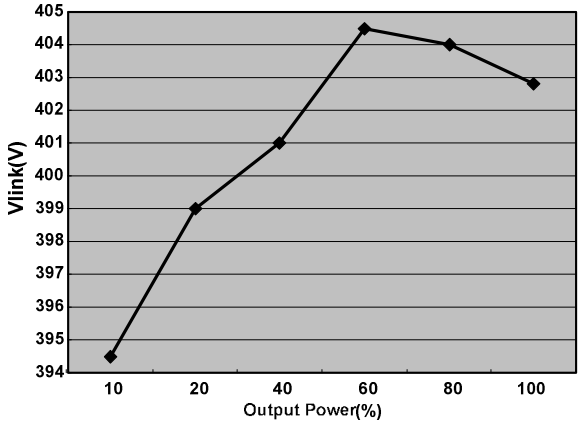

Fig. 6(d) Measured link capacitor voltage

5. Conclusion

In this paper, the new ZVZCS single-stage PFC AC/DC converter is proposed. By experimental results of an 85W converter, the operation principle and main features of the proposed converter are confirmed. Link capacitor voltage of the proposed converter could be sustained below 405V at no load and high line input conditions. Moreover the proposed converter met the harmonic regulations and had high efficiency. Therefore, the proposed converter can be expected to be widely used for low power applications such as laptop adapter.

Reference

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