새로운 커뮤테이션 기법을 갖는 단상 매트릭스 컨버터

최남섭*, 리위룽*, 한병문**, 노의철***, 고종선****
*전남대학교, **명지대학교, ***부경대학교,****단국대학교

Single Phase Matrix Converter with Novel Commutation Strategy

Choi Nam-Sup*, Li Yulong*, Han Byung-Moon**, Nho Eui-Cheol***, Ko Jong-Sun****
*Chonnam National University, **Myongji University, ***Pukyong National University,
****Dankook University

ABSTRACT

In this paper, a single phase matrix converter circuit with novel commutation technique is proposed. With commercial IGBT modules, the proposed converter is quite compact in structure and easy to build. The applied commutation strategy introduces a simple RC circuit as commutation aid without need for sensing information, leading to stable and reliable operation. The modulation method is explained; the detailed commutation procedure is illustrated. Finally, the simulation results show the validity and verification of the proposed single phase matrix converter.

1. Introduction

Direct AC-AC converters based on matrix converter topology have received considerable researching interest in recent years, especially the three phase matrix converter. However, the single phase matrix converter has rarely been dealt with. The single phase matrix converter was first realized by Zuckerberger [1], there are also some works done by Xahirrudin in [2,3]. In this paper, with a smart arrangement of common-collector and common-emitter bidirectional switch structure, a single phase matrix converter circuit with four commercial available IGBT modules is built, leading to compact structure and relatively high power density.

In order to construct a reliable matrix converter, it is important to overcome the problem of commutation of the current path between the bidirectional switches. In the proposed converter, for commutation purpose, a simple RC circuit is added as commutation aid. With traditional dead time commutation technique applied, the operation is quite stable and robust.

In this paper, the modulation method in [3] is applied and reviewed; the commutation operation is described. Finally, simulation results support the validity and verification of the proposed converter circuit and commutation technique.

2. Sigle phase matrix converter circuit

Fig. 1 shows the practical circuit topology of a single phase to single phase matrix converter. As seen in Fig. 2, the converter mainly consists of four bidirectional switches. Namely, S_1-S_2, S_3-S_4, S_5-S_6, S_7-S_8 are noted as S_{a+}, S_{a-}, S_{b-} and S_{b+} respectively. S_{a+} and S_{b-} are of common emitter arrangement; S_{a-} and S_{b+} are of common collector structure. It also can be seen from Fig. 1 that in order to build such a converter, four commercial IGBT modules are needed. The modules are S_1-S_7, S_2-S_4, S_3-S_5, S_6-S_8. With these four IGBT modules smartly arranged, the circuit structure is very compact and the converter will be easy to build. Cf is input filter component, while L and R are loads. Extra elements C_{s1}, C_{s2}, R_{s1}, C_{s3}, C_{s4} and R_{s2} are added for commutation purpose. The gating signals for IGBTs are in the type of Pulse Width Modulation (PWM), and will be shown in Fig. 2. It should be noted that a short dead time t_d is inserted. The generation of gating logic will be quite simple.

3. Modulating formulation

The input voltage $v_s(t)$, output current $i_o(t)$, and fundamental output voltage $v_{ofun}(t)$ are given by

$$v_s(t) = V_s \sin(\omega_i t) = V_s \sin(\theta) \quad (1)$$

$$i_o(t) = I_L \sin(\omega_o t + \phi) \quad (2)$$

$$v_{ofun}(t) = V_o \sin(\omega_o t + \psi). \quad (3)$$

In order to explain the modulation strategy, it is necessary to look into a single switching period. This is quite the same with the analysis of conventional voltage source converters. Under the assumption that the switching frequency f_s is much higher than both input frequency f_i and output frequency f_o, it is reasonable to treat the input voltage as a constant value V_i in one switching period. Fig. 3 shows the input voltage, output voltage and output current waveform in one switching period. In Fig. 3, it is supposed that the instant input voltage has a positive value V_i. The output

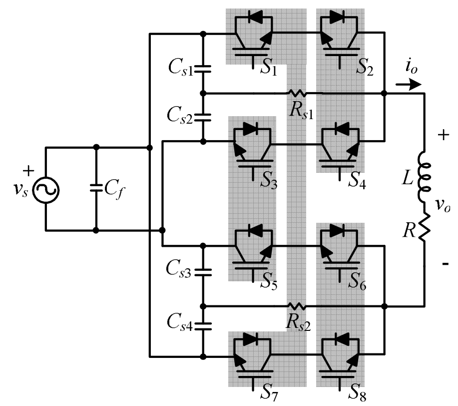

Fig. 1 Single phase matrix converter circuit topology

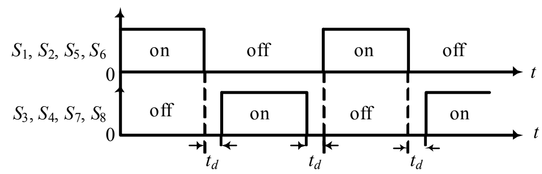

Fig. 2 IGBT gating signals

current is also assumed to be positive.

In the first subinterval $0-dT_s$, S_{a+} and S_{b-} are on, S_{a-} and S_{b+} are off. The output voltage v_o is equal to V_i. The circuit equations are

$$v_o = V_i \quad \left(0 < t < dT_s\right) \tag{4}$$

$$i_o = \frac{V_i}{L} \cdot e^{-\frac{R}{L}t} \tag{5}$$

In the second subinterval dT_s-T_s, S_{a+} and S_{b-} are off, S_{a-} and S_{b+} are on. The output voltage v_o is equal to $-V_i$. The circuit equations are

$$v_o = -V_i \quad \left(dT_s < t < T_s\right) \tag{6}$$

$$i_o = -\frac{V_i}{L} \cdot e^{-\frac{R}{L}t} \tag{7}$$

The averaged output voltage in one switching period will be

$$\bar{v}_o = \frac{1}{T_s}\int_0^{T_s} v_o(t)\,dt = \frac{1}{T_s}\left[dT_sV_i - (1-d)T_sV_i\right] = \left(d - d'\right)V_i \tag{8}$$

where $d=1-d$.

(8) defines the relationship between input and output. Recognizing $\bar{v}_o$ as the instant sampled value of (3), the duty

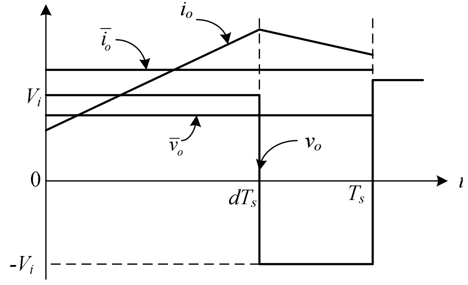

Fig. 3 Synthesis of output voltage

ratio d can be determined for every switching period.

In this case, the expression of (3) will be treated as a reference command. Let v_{oref} be the instant output command, then consider (8) again, (9) can be obtained,

$$v_{oref} = \left(d - d'\right)V_i. \tag{9}$$

In (9), V_i can be obtained by simultaneously sensing the input voltage through peripheral sensing circuit. Let v_{isen} be the instantly sensed value of input voltage, then (9) can be written in (10),

$$d - d' = \frac{v_{oref}}{v_{isen}} = q. \tag{10}$$

Considering $d=1-d$, the duty ratio for IGBTs can be finally calculated as

$$d = \frac{1+q}{2}, \quad d' = \frac{1-q}{2}. \tag{11}$$

It is obvious that

$$0 \le d, d' \le 1. \tag{12}$$

Equivalently,

$$|q| \le 1. \tag{13}$$

(13) must exist for any time t, and this implies the input and the output wave forms must be synchronized and the fundamental of output voltage must cross zero more frequently than the input voltage. Hence, the single phase matrix converter will be a frequency step-up converter. The relation of input frequency f_i and output frequency f_o will be

$$f_o = r \times f_i, \quad \text{where } r = 1,2,3\ldots \tag{14}$$

Based on the previous derivation, the switching pattern can be concluded and the four bidirectional switches will be controlled according to this pattern.

4. Commutation procedure

In order to explain the commutation procedure, the upper circuit branch containing S_1, S_2, S_3 and S_4 will be treated as an example. It is assumed that the load current I_o flows in the direction shown in Fig. 1. Fig. 4 illustrates the commutation procedure. The bold line in Fig. 4 is used to show current path.

Mode I is the initial state. S_1 and S_2 are off, S_3 and S_4 are on. Load current Io flows through D_3-S_4. Then dead time begins, all the switches are turned off. Mode II will be the circuit state. Since C_{s1} and C_{s2} imply same impedance, I_o will separate equally through C_{s1} and C_{s2}. Hence, C_{s1} and C_{s2} will be both charged. When dead time ends, S_1 and S_2 will be turned on, Mode III starts. I_o commentates to S_1-D_2 path. C_{s1} discharges and C_{s2} charges towards V_s. After the capacitors finishing charging and discharging, Mode IV is the final state, I_o flow through S_1-D_2.

Fig. 5 shows the reversed commutation procedure. Mode 1 is the initial circuit state. It is the same with Mode IV in Fig. 4. S_1 and S_2 are on, S_3 and S_4 are off. I_o flows through

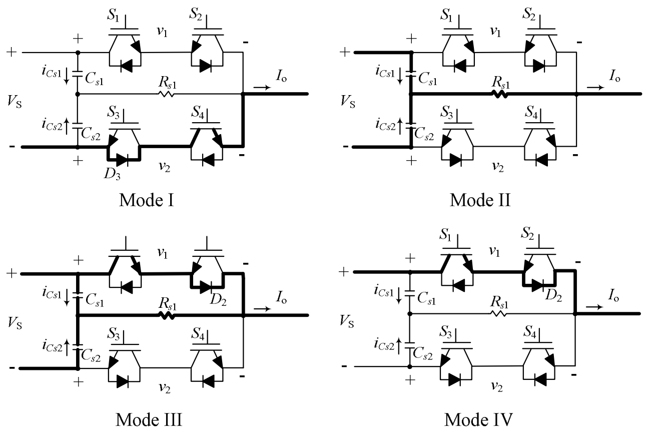

Fig. 4 Commutation procedure (Set I)

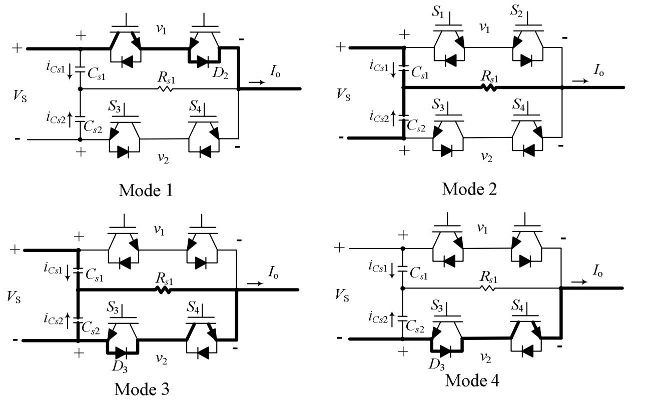

Fig. 5 Commutation procedure (Set II)

S_1-D_2. Then dead time begins and all the switches are turned off and Mode 2 begins. I_o will also equally separate and flow through C_{s1} and C_{s2}. Circuit enters Mode 3 after dead time ends. I_o commutates to D_3-S_4. Finally, after the capacitors finishing charging and discharging, Mode 4 is the last state. I_o flows through D_3-S_4.

With a simple RC circuit added as commutation aid, the commutation operation dose not require any sensed circuit information, leading to stable and reliable operation.

5. Simulation

In order to verify the operation of the designed single phase matrix converter, simulation is performed on PSIM platform. The circuit parameters are

V_s=100V, L=5mH, R=2.5Ω, f_s=5kHz,
R_s =4.7Ω, C_s=0.22F, t_d=0.5μs.

Fig. 6 and Fig. 7 show the simulation result when output frequency f_o=120Hz. It can be seen in the simulation figures that the designed single phase matrix converter operates well.

5. Conclusions

In this paper, single phase matrix converter is treated. With smart arrangement of four IGBT modules, the circuit is quite simple and compact. The converter utilizes dead time

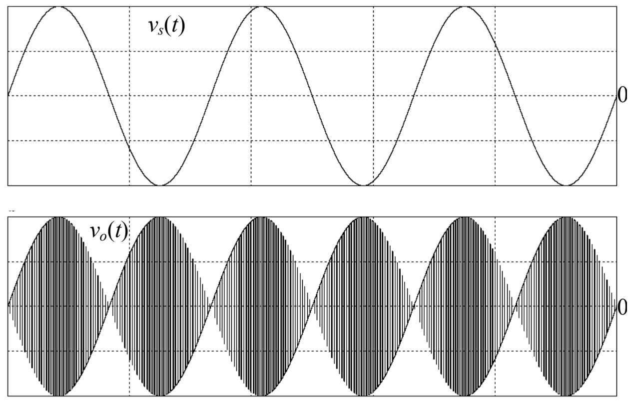

Fig. 7 Simulation results when f_o=120Hz
($v_s(t)$: 50V/div, 10ms/div; $v_o(t)$: 50V/div, 10ms/div)

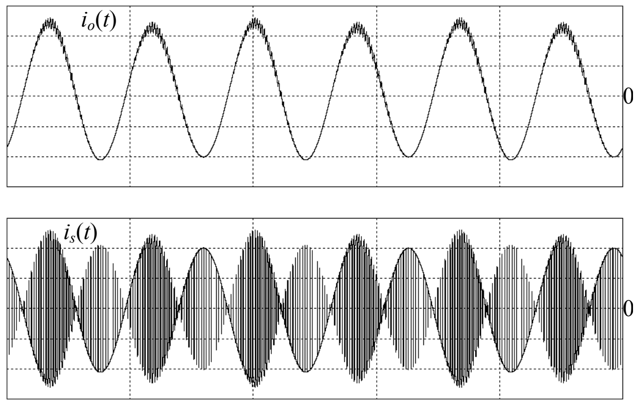

Fig. 8 Simulation results when f_o=120Hz
($i_o(t)$: 5A/div, 10ms/div; $i_s(t)$: 5A/div, 10ms/div)

commutation with RC commutation aid added, leading to stable and reliable operation. The modulation strategy is described. Commutation operation is also illustrated. Simulation results show the verification of the designed converter.

Acknowledgement

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