The study of the Asymmetrical Half-Bridge Converter With magnetic coupled post regulator

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Abstract

In this paper, a multiple-output converter using a coupled-inductor is proposed. The Asymmetrical Half-Bridge Converter (AHBC), which is used as a master converter, obtains ZVS in the primary side switches. For the tight output voltage regulation of the slave output, the Secondary Side Post Regulator (SSPR) is adopted. The proposed magnetically coupled output filter inductor reduces the number of semi-conductor devices and magnetic components. Also, the circuit enables ZCS off switching in the SSPR MOSFET and rectifying diodes. The modes of operation which are caused by the coupled-inductor and post regulator are explained. The analyzed modes of operation of the proposed multiple-output converter are verified by the simulation and experimental results.

1. Introduction

As the analog and digital electronics become more complicated and advanced, they require several voltage sources in one electronics system. For the industrial demand, a number of DC/DC converters are required in the system and these converters increase the overall system cost, size and complexity. To deal with these challenges, various multiple-output approaches have been proposed [1]-[3]. As the system requirement for each output regulation specification becomes tighter, the cross-regulation may not be feasible, especially for a wide varying load conditions. Therefore a post regulator scheme should be used in a multiple-output converter to overcome the limitations of the cross-regulation [4] [5].

In this paper, a post regulator scheme using a coupled-inductor, as shown in Fig.1, is proposed. It reduces the number of magnetic cores through the integration of the output inductor. The freewheeling diode in the conventional circuit is removed because the inductor (or switch) current became zero before S_3 turns off. By properly controlling the switch timing, the SSPR switch can achieve ZCS turn on and ZCS turn off through the fast current commutation in the transformer, T_2, without effective duty loss. As a master power stage, the AHBC is used for its inherent soft switching in the MOSET and the clamped switch voltage as were described in [6]-[7].

2. Analysis of the proposed converter

2.1 The modes of operation

The operation of the proposed converter, shown in Fig.2, is analyzed. For the slave output regulation, a buck type with tailing edge modulation is used. To simplify the steady state analysis several assumptions are made; (a) Switches S_1, S_2, S_3 are ideal except for the parasitic capacitances C_1, C_2 and body diodes D_{S1} and D_{S2}. (b)V_{O1} and V_{O2} are constant during the switching period.

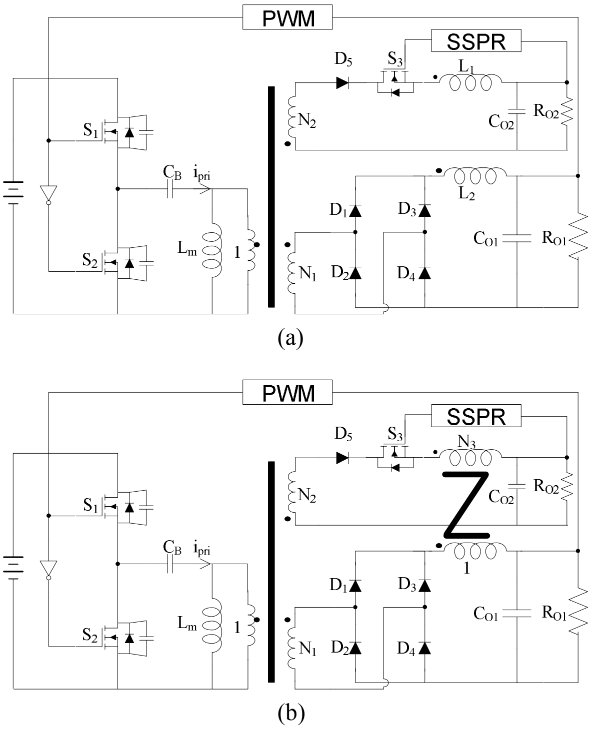


Fig. 1 The circuit configuration of the multiple-output converter
(a) Conventional circuit. (b) Proposed circuit.

(c) The ideal transformers with leakage and magnetizing inductances are modeled for T_1 and T_2. The sub-fix of the voltage and current follows the corresponding component names.

Mode1 [t_0~t_1]
During Mode1, S_1 is on and S_2, S_3 are off. i_1 flows through D_1, D_4 and L_{m2}, which is magnetizing inductance of T_2. During this mode, the slave part is blocked by D_5 and thus no energy is transferred. The currents are expressed in (1)-(2).

$$i_1(t)=\frac{(N_1(1-D)V_g - V_{O1})}{L_{m2}}t,\ i_{m1}(t)=\frac{(1-D)V_g}{L_{m1}}t, \quad (1)$$

$$V_{lm2}(t)=(N_1(1-D)V_g - V_{O1}) \quad (2)$$

Mode2 [t_1~t_2]
During Mode2, the S_2 voltage becomes zero and the primary side current of the transformer changes its direction

Mode3 [t_2~t_3]
Mode3 starts when S_2 is turned on. The current i_1 flows through D_2, D_3 and L_{m2}. The slave part is blocked by S_3. The current

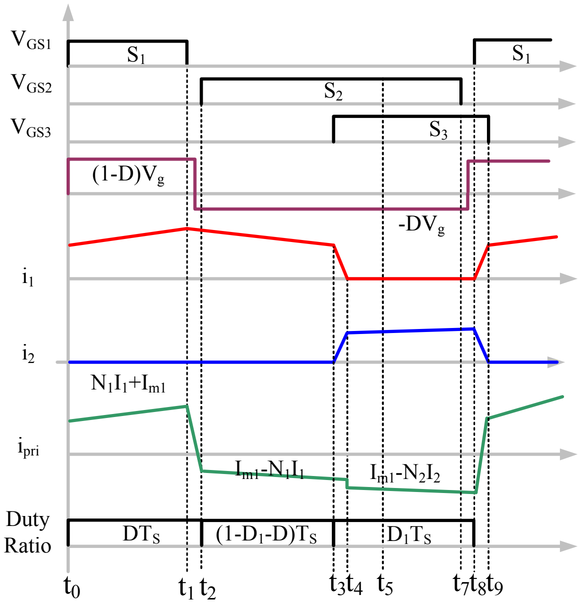


Fig. 2 The operating waveforms

equations are shown in (3).

$$i_1(t)=\frac{N_1DV_g-V_{O1}}{L_{m2}}t,\ i_{m1}(t)=\frac{-DV_g}{L_{m1}}t \tag{3}$$

Mode4 [t_3~t_4]

Mode4 begins when S_3 is turned on. The current i_2 starts to increase and current i_1 decreases. In this mode, i_1 and i_2 flow to the T_2 terminal simultaneously and then the voltage and current of the both sides of the T_2 affects each other. The related equations are expressed in (4)-(5). The winding voltage of the T2 is exhibited in (6)

$$i_1(t)=(N_1DV_g-V_{lm2}-V_{O1})t/L_{lk1},\ \ i_{lm2}(t)=V_{lm2}t/L_{m2} \tag{4}$$

$$i_2(t)=(N_2DV_g-N_3V_{lm2}-V_{O2})t/L_{lk2},\ \ i_1(t)=i_{lm2}(t)-N_3i_2(t) \tag{5}$$

$$V_{lm2}(t)=\left(\left(\frac{N_1}{L_{lk1}}+\frac{N_2N_3}{L_{lk2}}\right)DV_g-\frac{V_{O1}}{L_{lk1}}-\frac{N_3V_{O2}}{L_{lk2}}\right)t\Big/\left(\frac{1}{L_{m2}}+\frac{1}{L_{lk1}}+\frac{N_3^{\,2}}{L_{lk2}}\right) \tag{6}$$

Mode5 [t_4~t_5]

Mode5 starts when i_1 becomes zero. D_2 and D_3 are turned off softly as i_1 goes to zero. The peak current of the SSPR switch is the same as the reflected magnetizing current and the averaged value during one switching period becomes the slave output load current. The current equations during this mode are shown in (7)

$$i_2(t)=\frac{(N_2DV_g-V_{O1})}{N_3^{\,2}L_{m2}}t,\ i_{m2}(t)=i_2(t) \tag{7}$$

Mode6 [t_5~t_6]

During Mode6, the S_1 voltage becomes zero and the primary side current of the transformer T_1 changes its direction.

Mode7 [t_6~t_7]

This mode starts when S_1 is turned on. Due to the positive terminal voltage of the T_1, the rectifying diodes D_1 and D_4 are turned on. The current commutation seen from mode4 occurs again. The voltage and current equations are similar to (4)~(6) except the voltage of the leakage inductance in T_2. The ZCS off in the SSPR switch can be obtained by turning off S_3 after i_2 goes to zero.

2.2 The steady-state analysis

Utilizing the results of the modes of operation, a voltage conversion ratio is obtained. The averaged (or DC) voltage and current are required to design the proposed converter properly. Short-time and transient mode are neglected to simplify the analysis. The averaged magnetizing currents are calculated in (8)~(11) by applying the charge-balance condition in the output capacitor (C_{O1}, C_{O2}) and the DC blocking Capacitor (C_b).

$$(<i_{m2}>-I_{O1})(1-D_1)T_S+(-I_{O1})D_1T_S=0,\ \Rightarrow\ <i_{m2}>\cdot(1-D_1)=I_{O1} \tag{8}$$

$$-I_{O2}(1-D_1)T_S+(<i_{m2}>/N_3-I_{O1})D_1T_S=0 \tag{9}$$

$$<i_{m2}>\cdot D_1=N_3I_{O2},\ <i_{m2}>=I_{O1}+N_3I_{O2} \tag{10}$$

$$<i_{m1}>=\left(N_1(1-2D)+D_1(N_2/N_3-N_1)\right)\cdot\left(I_{O1}+N_3I_{O2}\right) \tag{11}$$

From (10) and (11), the two output voltage relations can be derived as in (12)

$$\left(I_{O1}+N_3I_{O2}\right)\cdot D_1=N_3I_{O2},\ \Rightarrow\ V_{O2}/V_{O1}=D_1R_{O2}\big/N_3(1-D_1)R_{O1} \tag{12}$$

$$where\ I_{O1}=V_{O1}/R_{O1},\ I_{O2}=V_{O2}/R_{O2}$$

Applying the power balance condition of the input terminal and the sum of output terminals in (13), the voltage conversion ratio from the input to the master part can be derived as (14).

$$V_g\cdot<i_{in}>=V_{O1}\cdot<i_1>+V_{O2}\cdot<i_2> \tag{13}$$

$$\frac{V_{O1}}{V_g}=\frac{2N_1D(1-D)+DD_1(N_2N_3-N_1)}{(1-D_1)+D_1^{\,2}R_{O2}\big/(1-D1)R_{O1}} \tag{14}$$

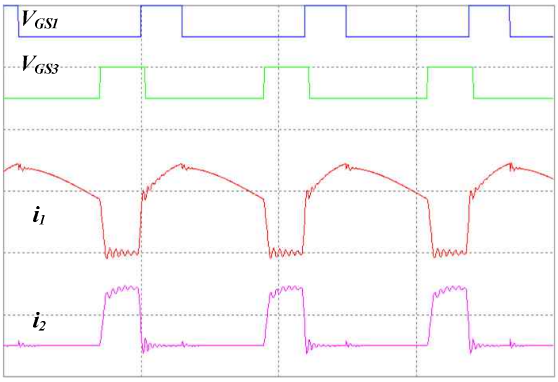
3. Experimental Result

The proposed converter was simulated and implemented to verify the concept and theoretical analysis. The converter is tested under 400V input voltage and switching frequency F_S is 70kHz. The output voltage and currents of the converter are specified as V_{O1}=170V, I_{O1}=1.8A in the master output and V_{O2}=70V, I_{O2}=1A in the slave output. From the converter voltage gain, the normalized turns ratio are selected as N_1=1, N_2=1.4, N_3=0.5. The other circuit parameters and hardware components are summarized in table 1.

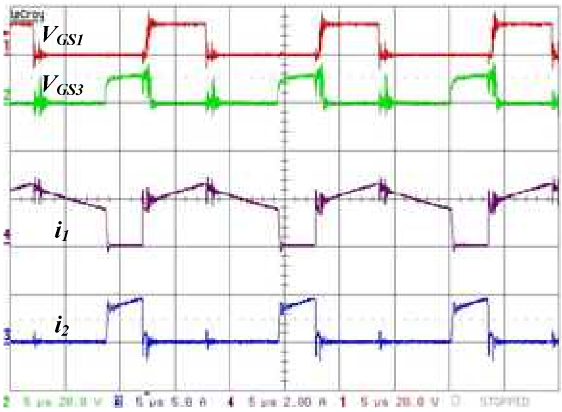
The operation of the proposed circuit through the computer simulations, as shown in Fig.3, is similar to that the experimental results. The current of the switch in the post regulator starts from zero because the current commutation in T_2. When switch of the primary side is turned off, the reversed voltage in the primary side of the T_2 causes the current commutation. The S_3 should be turned off after current becomes zero for the ZCS off.

Table1. Circuit parameters

Component	Value	Component	Value
C_b	100nF/15uF	L_{m1}	406uH
C_{O1}/C_{O2}	2mF/1mF	L_{m2}	340uH
S_1,S_2	SWT20NM50	D_1-D_5	FSF10A60
S_3	IRFB33N15D	Core	EER4950S/EI50



(a) Simulation result



(b) Experimental result

Fig.3 Currents of the auxiliary transformer in steady-state

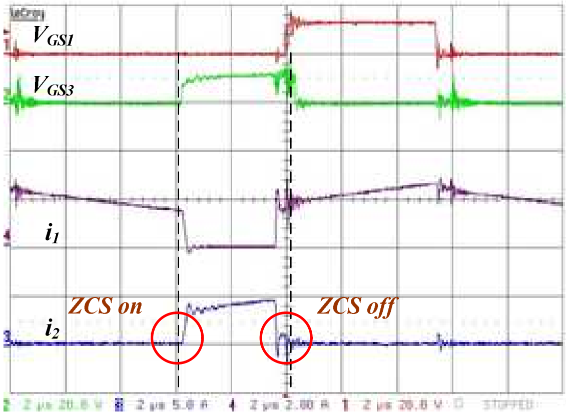


Fig.4 ZCS on and ZCS off of the SSPR switch

4. Conclusion

A multiple-output converter using the SSPR with a coupled-inductor is proposed. To reduce the size and overall cost, the output filter inductor of the SSPR is integrated to the master part filter inductor. The proposed converter achieves ZCS on and off in the SSPR switch. The ZCS off in the SSPR switch eliminates the freewheeling diode in the slave part. Also the current of the rectifying diodes are turned off softly. The modes of operation of the proposed converter are analyzed to obtain the design equations. 370W prototype hardware is built to verify the analysis.

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