Digital State Feedback Control for a Single/Parallel Module Buck Converter Using the Pole Placement Technique

Hyun-Su Bae, Jeong-Hwan Yang, Jae-Ho Lee and Bo-Hyung Cho

School of Electrical Engineering, Seoul National University
Gwanak P. O. Box 34, ENG420-043, Seoul, 151-744, KOREA

Abstract

In this paper, a simple digital control scheme for the single/ parallel module buck converters is proposed using a digital state feedback control method. The discrete state feedback controller structure for the robust tracking control is derived by using the error state. The proposed control system can precisely achieve the interleaved current sharing and the output regulation, and can achieve the systematical controller design for a given converter specification using the pole placement technique. For a design example, the single module buck converter is simulated using the MATLAB Simulink software and two 100W parallel module buck converters with a TMS320F2812 DSP is implemented.

1. Introduction

Ever increasing demands for the development of compact, lightweight power supplies with more power density, higher efficiency and fast dynamics, often require power conversion through parallel connected converters. In order to configure the parallel module converter, a current mode controller is needed to share an equal current among the converter modules. Digital control offers the potential advantages of immunity to analog component variations, programmability and possibilities to improve performance using more advanced control algorithms.[2] However, digital current mode control for the parallel module converter is not easy because the switch or inductor current is a fast-changing waveform and the switching frequency is high. State feedback controls for DC-DC converters have been proposed for the systematical controller design.[3,4] However, these methods for parallel module converters are very complex and the expansion of converter modules is not convenient because the controller design is performed with a high order state and multi-input system.

In this paper, a simple digital control scheme for the single /parallel module buck converters is proposed using a digital state feedback control method. For the single module control, the discrete state feedback controller structure for the robust tracking control is derived by using the error state. For the parallel module control, the two loop control scheme using a similar concept of the single module control is applied. In this approach, the inner current loop changes a multi-input/multi-output system into a single-input/single-output system. This method can precisely achieve the interleaved current sharing among the converter modules and can achieve the output voltage regulation for the single/parallel module converters. Also, the proposed method can achieve the systematical controller design for digital implementation using the pole placement technique. For a design example of the proposed control scheme, the single module buck converter is simulated using the MATLAB Simulink software and a parallel module bus regulator (buck converter) in the LEO satellite power system application, which has an constant solar array voltage regulated by a solar array regulator, is implemented using a TMS320F2812.

2. Robust Tracking Control using the Pole Placement Technique

2.1 The state feedback controller structure in the discrete time domain

Most switching converters operating in the continuous conduction mode (CCM) have two state equations within the one switching period as follows;

$$\begin{aligned} \dot{x}(t) &= A_1 x(t) + b_{vg1} v_g(t) + b_{io1} i_o(t), \quad nT_s < t < (n+d)T_s \\ \dot{x}(t) &= A_2 x(t) + b_{vg2} v_g(t) + b_{io2} i_o(t), \quad (n+d)T_s < t < (n+1)T_s \end{aligned} \tag{1}$$

where, $x(t)$ is a state vector, $v_g(t)$ is an input voltage, $i_o(t)$ is an output current, $d(t)$ is a duty ratio and T_s is a switching period. From the continuous difference equation (1), the average discrete time state equation can be derived for the discrete state feedback controller.[1]

$$\begin{aligned} x(k+1) &= A_z x(k) + B_z d(k) + B_{vgz} v_g(k) + B_{ioz} i_o(k) \\ y(k) &= C_z(k) \\ \text{where } A_z &= \exp(A_1 D T_s)\exp(A_2 D T_s) \\ B_z &= A_z\left[(A_1 - A_2)X + (B_{vg1} - B_{vg2})V_g + (B_{io1} - B_{io2})I_o\right] \\ B_{vgz} &= (DB_{vg1} + D'B_{vg2})T_s, \; B_{ioz} = (DB_{io1} + D'B_{io2})T_s \end{aligned} \tag{2}$$

where, X, $\mathrm{V_g}$ and I_o are the steady state value of the state, input voltage and output current, respectively. The objective is to design an overall system such that the output $y(k)$ will track asymptotically any step reference input, $r(k) = R$ (constant) , even with the presence of an input disturbance and with plant parameter variations. Let an error state, $e(k)$, and augmented state variables, $z(k)$, $u(k)$, $w(k)$, be defined and assume that the input voltage, v_g , and output current, i_o , are sustained and slowly varying.

$$\begin{aligned} e(k) &= r(k) - y(k) = R - C_z(k), z(k) = \dot{x}(k) \cong \frac{x(k+1) - x(k)}{T_s} \\ u(k) &= \dot{d}(k) \cong \frac{d(k+1) - d(k)}{T_s}, \; \dot{e}(k) \cong -C_z z(k) \\ w_1(k) &= \dot{v}_g(k) \cong 0, \; w_2(k) = \dot{i}_o(k) \cong 0, \text{ using Euler's method} \end{aligned} \tag{3}$$

Then the system can be expanded by the augmented state vector $\begin{bmatrix} e(k) & z(k) \end{bmatrix}^T$.

$$\begin{bmatrix} e(k+1) \\ z(k+1) \end{bmatrix} = \begin{bmatrix} 1 & -T_s C_z \\ 0 & A_z \end{bmatrix} \begin{bmatrix} e(k) \\ z(k) \end{bmatrix} + \begin{bmatrix} 0 \\ B_z \end{bmatrix} u(k), u(k) = -\begin{bmatrix} K_1 & K_2 \end{bmatrix} \begin{bmatrix} e \\ z \end{bmatrix} \tag{4}$$

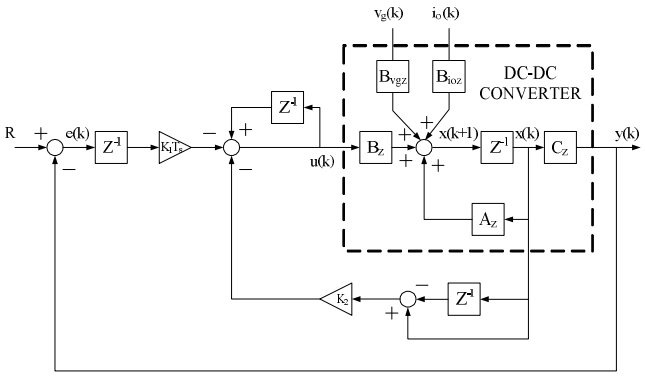

Fig. 1 The state feedback scheme for the robust tracking control

If the expanded system is controllable, then there exists a state feedback gain $\begin{bmatrix} K_1 & K_2 \end{bmatrix}$ such that the expanded system is stable. That means the output of the converters tracks the reference values. Furthermore, using the state feedback gain, the system's eigenvalues can be placed to the desired poles, which determine the performance of the feedback control system. Fig. 1 shows the overall closed loop system using the discrete state feedback control. The duty ratio can be derived from equation (3) and (4).

$$d(k) = d(k-1) - K_1 T_s e(k-1) - K_2[x(k) - x(k-1)] \tag{5}$$

Since the control input is the duty ratio, the magnitude of the control input must be checked because of its limitation. This can be easily checked from the allowed maximum duty ratio, the switching frequency, the designed feedback gain and the required system specification, as follows;

$$|u(k)| = |d(k)| = |K_1 R + K_2 x(k)_{spec}| < \frac{D_{\max} - D_{\min}}{T_s} \tag{6}$$

2.2 The single module buck converter design

The proposed discrete state feedback control scheme is applied to a single module buck converter as shown in Fig. 2. Using the un-terminated modeling method, the state equation of the buck converter is;

$$A_1 = A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix},\ b_{vg1} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \& b_{vg2} = \begin{bmatrix} 0 \\ 0 \end{bmatrix},\ b_{io1} = b_{io2} = \begin{bmatrix} 0 \\ \frac{1}{C} \end{bmatrix} \tag{7}$$

Employing equation (2)-(4), the augmented discrete state equation can be derived as a third order system. Thus, using the dominant pole approach for the pole placement technique, the desired pole locations can be easily obtained relating the given specification and the general second order system's response.

$$\text{Settling time} \cong -\frac{4T_s}{\ln(r)} \le \tau_{spec}$$

$$\text{Percent overshoot} \cong 100\exp\left(\frac{\ln(r)}{\theta}\pi\right) \le P.O._{spec} \tag{8}$$

$$z_{desired} = r\angle \pm\theta = r\cos(\theta) \pm jr\sin(\theta) \text{ and } r\cos(\theta)^{10}$$

To verify the theoretical analysis, the proposed discrete state feedback control scheme has been simulated with the MATLAB Simulink software: $L = 100\mu H$, $C = 100\mu F$ & $f_{sw,sample} = 100kHz$. From equation (8), the feedback gain is designed as

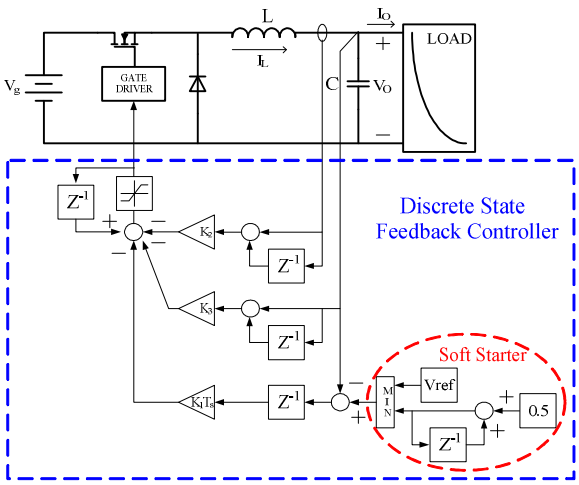

Fig. 2 The proposed single module buck converter control system

$$K_1 T_s = -0.0328,\ K_2 = 0.1554,\ K_3 = 0.3765.$$
$$(\text{where } \tau_{spec} = 300\mu\text{sec},\ P.O._{spec} = 1\%) \tag{9}$$

Fig. 3 shows the performance of the proposed control system when the step load is changed from 200W to 160W (20% load variation). It is observed that the system meets the required dynamics for the given settling time specification. Also, the soft starter and saturation function are included in the algorithm for a smooth transient without inrush current during a startup.

3. The Parallel Module Interleaved Buck Converter Design

The proposed digital control scheme using the parallel module buck converter is illustrated in Fig. 4. When the converter module is expanded, the system has a high order state and multi input, For example, the system as shown in Fig. 4, has three state variables and two independent input duty ratios and it makes difficult to design a state feedback controller. Furthermore, whenever the converter module is expanded, the redesign of whole controllers is always required. Thus, in order to perform the systematical controller design for the parallel module system, it is necessary to make a simple state feedback algorithm.

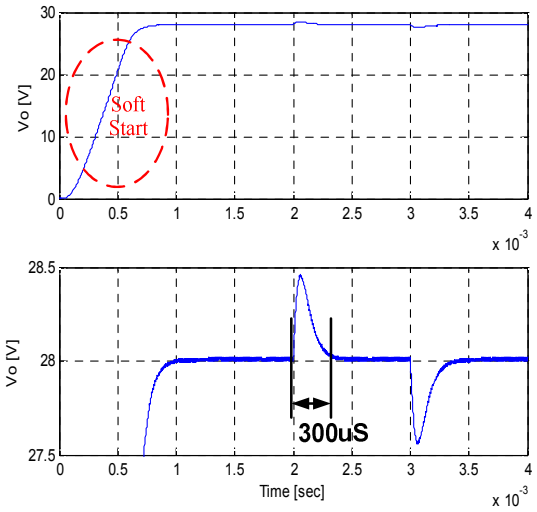

Fig. 3 The simulation results of the single module buck converter control

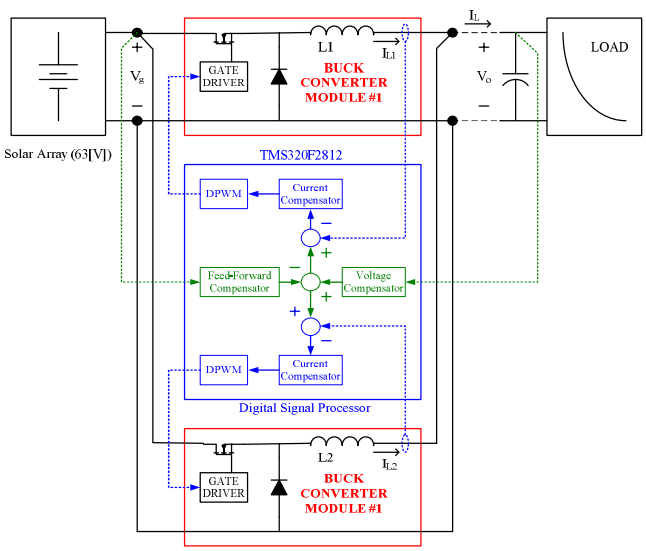

Fig. 4 The parallel interleaved buck control system

First, the inner current loop controller is designed for the each converter module, which has only one state variable, the inductor current, as shown in Fig. 4. Using the un-terminated modeling method, the state equation is derived and the discrete state equation employing equation (2) becomes

$$\dot{i}_{L,i}(t) = \frac{1}{L_i}\left[d(t)v_g(t) - v_o(t)\right], i_{L,i}(k+1) = i_{L,i}(k) + \frac{V_g T_s}{L_i} d(k) \quad (10)$$

where, input voltage and output voltage are assumed the sustained during one switching period, and $i = 1,2,\Lambda\ ,n$ is the number of converter modules. Let the control duty ratio be $d_i(k) = K_c[I_{ref} - i_{L,i}(k)]$, which is the proportional type state feedback controller in order to achieve the current sharing. Thus, the current closed system is a first order system as follows;

$$i_{L,i}(k+1) = \left(1 - \frac{V_g T_s K_c}{L_i}\right) i_{L,i}(k), K_c = \frac{L}{V_g T_s}\left(1 - \exp\left(-\frac{4T_s}{\tau_{spec}}\right)\right) \quad (11)$$

where, $L_i \cong L$ and K_c is a feedback gain using the general first order system's response. In this case, although a steady state error for a reference exists, the current sharing can be achieved. For this analysis, the ESR of the inductor, $r_{L,i}$, is considered and the final value theorem of the average large signal converter model (10) is used as follows;

$$\dot{i}_{L,i}(t) = -\frac{r_{L,i} + V_g K_c}{L_i} i_{L,i}(t) + \frac{V_g K_c I_{ref} - V_o}{L_i},\ v_g \cong V_g, v_o \cong V_o$$
$$i_{L,i}(\infty) = \lim_{s\to 0} s I_{L,i}(s) = \frac{V_g K_c I_{ref} - V_o}{r_{L,i} + V_g K_c} \cong I_{ref} - \frac{D}{K_c}(r_{L,i} << V_g K_c) \quad (12)$$

It is confirmed that the steady state inductor current is not related to the inductance, and the effect of ESR can be ignored. Thus, the proposed current loop can achieve the current sharing. The state equation of the output capacitor is derived to design the outer voltage loop from Fig. 4.

$$\dot{v}_o(t) = \frac{i_L(t)}{C} - \frac{i_o(t)}{C}, v_o(k+1) = v_o(k) + \frac{T_s}{C} i_L(k), i_L = \sum_{i=1}^{n} i_{L,i} \quad (13)$$

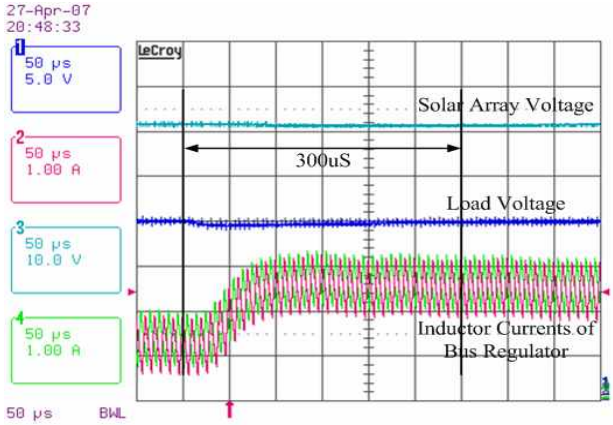

Fig. 5 The parallel converter control system response during load step

After closing the current loop, the parallel module converter becomes a SISO system, which has one control input, I_{ref}, and one output, i_L. Thus, the new power stage equation, which is terminated to the output capacitor, can be derived as

$$\begin{bmatrix} i_L(k+1) \\ v_o(k+1) \end{bmatrix} = \begin{bmatrix} 1 - \frac{V_g T_s K_c}{L_{eq}} & 0 \\ \frac{T_s}{C} & 1 \end{bmatrix} \begin{bmatrix} i_L(k) \\ v_o(k) \end{bmatrix} + \begin{bmatrix} \frac{V_g T_s K_c}{L_{eq}} \\ 0 \end{bmatrix} I_{ref}(k) \quad (14)$$

where, $L_{eq} = L/n$. Using the same procedure with the single module buck converter, the outer voltage regulation loop can be designed. The proposed digital state feedback control scheme has been tested with the prototype hardware whose schematic is shown in Fig. 4: $V_o = 20V, C = 200\mu F, L_1 \approx L_2 = 100\mu F, f_{sw} = 100kHz$ with the given specification of equation (9). Fig. 5 shows the converter behavior in the presence of a stepped load variation. It is observed that the voltage regulation as well as the interleaved current sharing is achieved during the transient period, as well as steady state. The response is in good agreement with specifications.

4. Conclusion

A simple digital state feedback control approach using the pole placement technique is proposed. Since the analysis and design is performed in the time domain using the state equation, the controller can be systematically designed for the required system specification. The proposed control system can achieve the interleaved current sharing and the output voltage regulation for the single/parallel module buck converters.

Acknowledgment

This study is partly supported by Korea Aerospace Research Institute (KARI).

Reference

[1] D. J. Packard, "Discrete Modeling and Analysis of Switching Regulator," Ph. D., California Institute of Technology, 1976

[2] Y. Duan and H. Jin, "Digital Controller Design for Switch Mode Power Converter," IEEE APEC 1999, Vol. 2, pp. 976-973.

[3] F. H. F. Leung, P. K. S. Tam and C. K. Li, "The Control of Switching dc-dc Converters-A General LQR Problem," IEEE Trans. on Industrial Electronics, Vol. 38, No. 1, Feb. 1991.

[4] C. C. Fang and E. H. Abed, "Output Regulation of DC-DC Switching Converters Using Discrete-Time Integral Control," American Control Conference, 1999, Vol. 2, pp. 1052-1056.