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Si-nanocrystalline nonvolatile floating gate memory device based on Schottky Barrier Tunneling Transistor

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Si-nanocrystal as discrete floating gate in nonvolatile MOSFET memory devices has been extensively investigated. Recently, Schottky Barrier Tunneling Transistor (SBTT) have been proposed as an alternative to traditional MOSFETs for sub-100 nm integration because of excellent scaling properties and ease of fabrication. SBTT is attractive for silicon-on-insulator (SOI) MOSFET because the parasitic resistance of source and drain is reduced.

We have fabricated the nonvolatile floating gate memory device with Si-nanocrystal based on Schottky Barrier Tunneling Transistor. The fabrication processes began with the <100> p-type silicon substrate (14~24 Ωcm). A thin tunnel oxide (~5 nm) was grown by dry oxidation and then a layer of uniform Si-nanocrystal dots with a FWHM of 6±1nm and a density of $7x10^{11}cm^{-2}$was deposited by a digital gas-feeding method in the LPCVD process.[1] Then the control oxide was deposited 30 nm thick SiO_2 using LPCVD at 400 ℃, and the gate electrode was deposited highly phosphorus doped n-type polycrystalline silicon. Erbium silicide in the source/drain was grown by RTA process after Erbium was sputtered and non-reacted erbium removed by wet etch in Sulphuric-acid hydrogen Peroxide Mixed (SPM) solution.

In our work, we investigated the electrical characteristics of memory device. A significant threshold voltage shift of fabricated floating gate memory devices based on SBTT was obtained due to the charging effects of Si-nanocrystal. But, the charge retention characteristic retained no good memory window width after 100 sec.

[References]

[1] Chan Park, Kyoungmin Kim, Eunkyeom Kim, Junghyun Sok, Kyoungwan Park, Moonsup Han, Materials science and engineering B, Volume 140, Issues 1-2, 25 May 2007, Pages 103-108