A Trend and the Developments of Low Dielectric Constant materials for Cu Integration

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As on-chip devices densities increase and active device dimensions are reduced, the signal delay and noise also increase due to capacitive coupling and crosstalk between the metal interconnections. Since signal delay, noise and power consumption all depend critically on the dielectric constant (k) of the separating insulator, much attention has recently been focused on replacing the standard silicon dioxide with new inter-metal dielectric materials that have considerably lower dielectric constants than that of thermal silicon dioxide films ($k = 3.9 \sim 4.2$). The fabricating technology of low-k materials for Cu/Low-k chips is essential to the next-generation Cu/Low-k device in which the low-k films with nano-pore structure is used for the inter-layer or the inter-metal dielectrics(IMD). The technology includes the High Density Plasma CVD(HDPCVD) method of low-k films, the HDPCVD method of a inter-metal barrier for integrating process, and various electrical and chemical, physical analysis methods for characterizing the fabricated dielectrics. Because low-k films with nano-pore structure for a next-generation of DRAM memory device of about $0.1\mu m$ or less must be fabricated by a series HDPCVD technologies, the prime point of our research is to the realization of low-k materials and process approximating ϵ_γ<2.0 on the basis of now immature SiOC composite film with nano-pore structure for the low-k CVD technologies, The many new resulting materials needs to be classified in terms of their materials characteristics, evaluated in terms of their properties, and tested for process compatibility. In addition, it addresses some of the needs for improved metrology for determining pore size, size distributions, structure, and mechanical properties.