Design Issues of Digital Display Interface

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Keywords: Display Interface, Clock Transmission, Clock and Data Recovery

Abstract

Depending on applications where transmission bandwidth, wire distance, power consumption and EMI environments vary, design trade-offs must be made to optimize the display interface. After introducing the digital display interface architecture, topics such as cost, EMI, signal integrity, scalability and content protection are discussed with available techniques. Implementation issues are discussed regarding their cost and design complexity. Existing standards are reviewed and comparison on their strengths and shortcomings are discussed.

1. Introduction

The required data bandwidth for display is ever increasing. This year, the size of the mainstream LCD monitor grew to more than 20 inches and the premium LCD TV panel supports more than 1 billion colors. Moreover, the refresh rate is about to double from 60 Hz to 120 Hz in order to reduce the motion blur problem of the LCD. Theses moves demand the improvement of the digital display interface.

In 1999, Digital Visual Interface (DVI) was introduced as the de facto standard of the digital display interface for a PC monitor. Now, there are many digital display interface standards which dominate in their own application areas. For instance, Low Voltage Differential Signaling (LVDS) is prevailing as the internal LCD panel interface, DVI is dominating as the external PC monitor interface and HDMI (High Definition Multimedia Interface) is capturing consumer electronics market. DisplayPort, the next generation of display interface, aims to unify all of these market sectors. These standards are competing against each other to extend their territory.

The competition of the digital video interface technology occurs not only on the transmission path from the graphic source to the display box, but also inside the display box. The so-called intra-panel interface, where a timing controller (TCON) and column drivers (LDIs) in the LCD panels are connected, RSDS and mini-LVDS are predominantly used. However, attempts are being made to replace Reduced Swing Differential Signaling (RSDS) and mini-LVDS with a new intra-panel interface with better performance.

In recent years, mobile displays have grown rapidly. The total production of mini-displays for handsets has already exceeded the total production of large displays for TVs and monitors. Since the size of handset display is also increasing for web-browsing, e-mail, and gaming, the improvement of handset displays is required as the history of large displays says. Two standards, MDDI that Qualcomm proposed and MIPI that Nokia proposed, are dominant players in this application.

2. Digital Display Interface Architecture

Modern display interfaces typically use small swing differential signaling and serialization. Though the basic architecture of a digital display interface is common and similar even to the architecture used in networks and IOs, such as PCI-Express, Serial AT Attachment (SATA) and Gigabit Ethernet, several differences among the standards still exist on the clock transmission scheme as shown in Fig. 1. For instance, LVDS and DVI transmit a pixel clock and DisplayPort transmits only the data stream.

In the bit clock transmission scheme bit clock is sent over to the receiver to sample every bit of the serial data stream. The receiver doesn't need to have a Phase-Locked Loop (PLL) or a Delay-Locked Loop (DLL) for clock generation. This architecture is relatively immune to jitter because the same amount of jitter appears at the clock lane and the data lane

The byte clock transmission scheme sends a byte clock to represent the byte boundary of original parallel data. In this scheme, the receiver usually adopts the DLL to generate multi-phase clocks to sample every bit of the serial stream. This architecture also has relatively good immunity to jitter. However, skew among clock and data, which occurs due to cable length difference, must be controlled and kept within a bound of less than a bit time.

Transmitting the reference clock is suitable for a

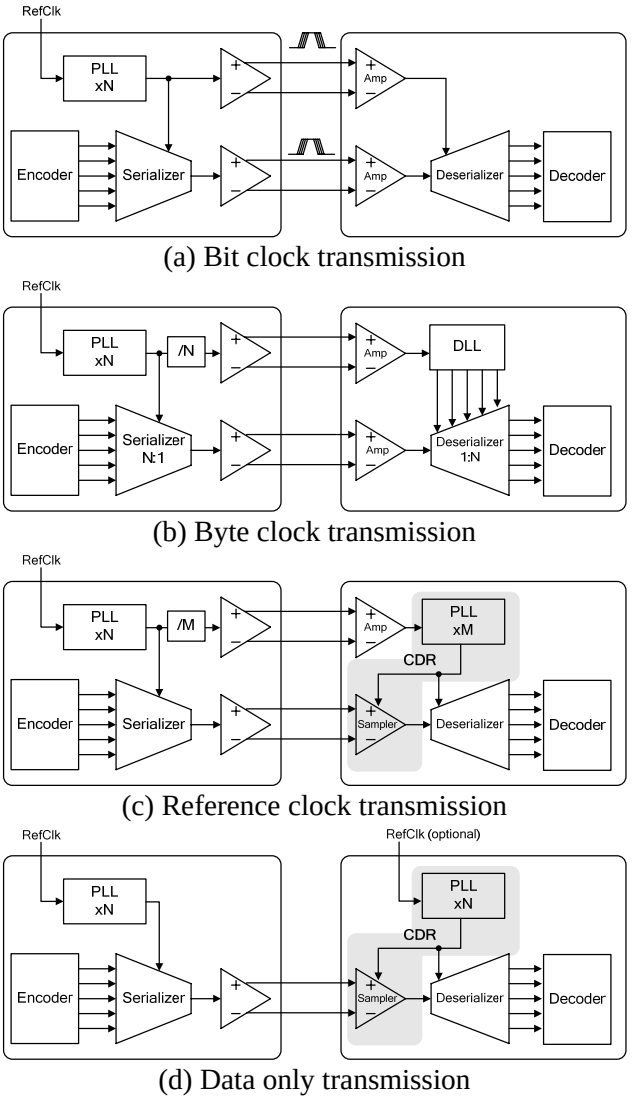

Fig. 1. Various clock transmission schemes.

high speed link because the receiver has a clock-and-data-recovery (CDR) circuit that obtains frequency-lock to the reference clock and gains phase-lock for sampling the bit stream. Since the byte boundary must be aligned in the receiver, a delimiter must be sent using a proper encoding scheme. Use of encoding offers many benefits such as allowing a large amount of skew among channels, maintaining DC-balance, and sending V-SYNC, H-SYNC, or other control signals using out-of-band characters. The scheme also covers a wide operating frequency range because frequency information is carried in the reference clock just as the byte clock transmission scheme.

The embedded clock scheme eliminates the clock and thereby reduces cost and eases EMI peaks in the clock. The scheme is typically used in the network physical layer such as PCI-Express, SATA, Gigabit Ethernet, and so on. In this scheme, the CDR circuit extracts the frequency information from the NRZ bit stream. The local reference clock with fixed frequency aids the CDR to obtain the frequency lock if its frequency is within hundreds of ppm of the target frequency. Since the link speed is fixed at the specified frequency, the link speed must be set at the maximum possible rate, but it can be wasted when the required data bandwidth is low.

3. Digital Display Interface Requirements

A. Cost

The cost is the most important factor because the production volume is huge and, thus, the price of display set drops rapidly. Also, the royalty issue is critical to overall cost of the system. Since the interface should be integrated using standard CMOS technology as an IP block, its chip are must be small. More importantly, the number of package pins and cables should be minimized.

B. EMI

ElectroMagnetic Interference (EMI) can be reduced by lowering the signal voltage level and the link speed. When the voltage margin and the speed requirement reach the limit, scrambling and spread spectrum techniques can reduce EMI further. Scrambling reduces EMI by eliminating repetitive patterns. A spread-spectrum clocking also reduces the EMI peak by spreading the peak spectral power to a wide frequency band by FM modulation. EMI issue is critical particularly in mobile display applications.

C. Signal Integrity

As the link speed increases, the bit time and, thus, the rise and fall times become shorter and the attenuation and impedance mismatch of the transmission line degrades the signal quality, limiting the transmission bandwidth. Impedance discontinuity due to via and stubs on circuit board and connectors incurs reflection. In multi-lane applications, crosstalk between lanes worsens signal integrity as well.

Signal integrity is critical particularly in the Flat Cable applications because the impedance of the cables is not as uniform as that of the PCB and poses a serious limitation in increasing the bandwidth in applications such as intra-panel interface or mobile display interface. The signal integrity worsens in intra-panel application where one transmitter (TCON) transmits data to many receivers (LDIs) in a so-called multi-drop configuration.

D. Scalability

The display interface must be forward compatible with the future generation displays. The standard must be able to accommodate any expanded bandwidth. By allowing a pixel clock with arbitrary frequency covering many display resolution, future generation displays can be accommodated with a higher-frequency pixel clock.

E. Content Protection

Content protection is the key functionality to widen the market of high definition (HD) display by protecting HD contents against piracy. While Digital Rights Management (DRM), the content protection policy in software level, exists, the protection in a hardware level can provide more solid protection. To meet the requests, HDCP and DPCP are suggested as the content protection policy for DVI and HDMI, and for DisplayPort respectively.

F. Other Features

HDMI and DisplyPort send the audio data as well to reduce the entanglement of wires in the back of AV devices. Also, it would be desirable to accommodate the low-rate transmission of IOs such as USB without using extra wires to the PC monitor. Moreover, bi-directional A/V electronics could require camera data or microphone data in a back channel. In this case, packetizing data can include any type of data with added logic complexity and data overhead.

4. Implementation Considerations

A. Clock and Data Recovery Circuits

As mentioned in section 2, clock and data recovery are needed in the reference clock transmission and the embedded clocking scheme. In implementing the CDR, two different techniques are typically used: tracking and blind over-sampling. With blind over-sampling, valid data are determined later by examining the over-sampled data. However, in the tracking CDR, the sampling phase is continuously adjusted to the optimum point by comparing the phases of the data and sampling clock in a feedback loop called PLL.

A blind over-sampling CDR needs only one PLL even if multiple transmitters and receivers are integrated [7]. No other analog circuitry except the PLL is necessary and the feed-forward architecture is more amenable to digital implementation. However, over-sampling ratio should be high enough to achieve low BER, because phase accuracy is determined by the over-sampling ratio.

The tracking CDR uses a phase detector to obtain an accurate lock to the received data stream. However, tracking CDR needs PLL or DLL per lane, not allowing any sharing among channels [8]. Because multiple PLLs integrated in one chip might interact with each other, the jitter performance can be degraded. Therefore, DLL-based CDR or PLL with a phase interpolator is preferred as the number of channels is increased.

B. Coding

An 8B10B coding scheme provides DC-balancing and provides special characters in the code space. Various standards using 8B10B coding take advantage of special characters during an idle period for byte synchronization, channel alignment, or frequency compensation.

DC balancing is indispensable for AC coupling that enables inter-operation among chips operating at various supply voltages. Byte synchronization is to find the byte boundary from a serial bit stream. It is usually done by detecting a comma character (K28.5) with a run length of 5 which is not found in a normal data stream. Channel alignment is done to adjust more than one bit skew in multiple-lane applications at the same time as byte synchronization.

The Transition Minimized Differential Signaling (TMDS) coding is similar to 8B10B coding and is used by the DVI and HDMI interfaces. It offers the 25% coding overhead, DC-balancing, and special characters just as 8B10B coding. The only difference is that it produces transition minimization to reduce EMI.

C. Pre-Emphasis

When the channel lacks bandwidth for data speed, ISI occurs during data transition and results in the reduced timing margin for sampling. In that case, boosting high frequency component of data stream can compensate the low-pass characteristics of the channel. This is called equalizing.

Equalizing can be done at the transmitter side, the receiver side, or both [9]. Equalizing at the receiver side requires complex circuitry, such as ISI measuring circuit and the tunable high frequency amplifier. On the other hand, the implementation of equalizing at the transmitter side is simpler. It requires only multi-level drivers, which can be implemented just by connecting multiple single-level drivers.

5. Comparison of Existing Interfaces

Table 1 summarizes the discussed issues about existing interface standards. The most recent DisplayPort offers the most functionality. In intra-panel applications, as the display size grows, the distance from TCON to LDI is increased causing EMI and signal integrity problems. RSDS and mini-LVDS are expected to be replaced due to the lack of required functionality as seen in Table 1 and thus a new standard is in order.

Although MDDI is a mobile serial interface that VESA accepted, it sill has not been widely accepted because the packetizing scheme is not transparent to existing parallel interfaces and needs re-development of software and hardware.

A clock edge modulated link [10] is a newly proposed interface for mobile applications which sends clock and data in a single differential pair. Using only a single pair of wires reduces power consumption, form factor and EMI. Also it requires only a simple DLL in the receiver side. However, the CEM link requires double channel bandwidth.

6. References

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TABLE 1. Comparison of existing interfaces

	LVDS	DVI	DisplayPort	RSDS	mini-LVDS	MDDI	CEM Link
Clock transmission	Byte clock	Reference clock	Embedded clock	Bit clock	Bit clock	Bit clock	Bit clock (CEM)
Number of Lanes	10	4 (single) / 7 (dual)	1~4	10/13/16 (multi-drop)	4~7 (multi-drop)	2/3/5/9	1
Bit rate per Lane	~945Mb/s	~1.65Gb/s	1.62 / 2.7Gb/s	(rising/falling time < 500ps)	(rising/falling time < 500ps)	~400 Mb/s	~270 Mb/s
Common mode Voltage	1.125~ 1.275 V	3.0~3.3V	0~3.6V	0.5~1.5V	1.0~1.4V	0.6 ~1.35V	0.6V
Swing level (differential)	0.25~0.45V	0.8~1.2V	0.4~1.2V	0.1~0.6V	0.3~0.6V	0.25 ~0.45V	0.16V
Pre-emphasis	No	No	3.5 / 6.0 / 9.5dB	No	No	No	No
AC coupling	No	No	Yes	No	No	No	No
Spread spectrum	No	No	30/33kHz 0.5% down -spreading	No	No	No	No
Scrambling	No	No	16bit LFSR	No	No	No	No
Scalability	No	No	Packet	No	No	Packet	No
Content Protection	No	HDCP	HDCP / DPCP	No	No	No	No
Clock-and-Data Recovery	DLL	CDR Required	CDR & FD Required	No	No	No	DLL
Coding	No	TMDS	8B10B	No	No	No	DC-balancing CEM