Electrical Characteristics of Bottom-Contact Organic Thin-Film-Transistors Inserting Adhesion Layer Fabricated by Vapor Deposition Polymerization and Ti Adhesion Metal Layer

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Abstract

The electrical characteristics of organic thin-film-transistor (OTFTs) can be improved by inserting adhesion layer on gate dielectrics. Adhesion layer was used as polymeric adhesion layer deposited on inorganic gate insulators such as silicon dioxide (SiO_2) and it was formed by vapor deposition polymerization (VDP) instead of spin-coating process. The OTFTs obtained the on/off ratio of ~10^4, threshold voltage of 1.8V, subthreshold slop of 2.9 V/decade and field effect mobility about 0.01 cm^2/Vs.

1. Introduction

In order to the advantage of low cost, flexibility, low temperature and large area processing, etc., organic thin-film transistors (OTFTs) have received global interest for more than a decade. Inorganic materials have been generally used as gate insulator, such as silicon oxide that has properties of a low electrical conductivity and a high breakdown field. However, inorganic insulating layers, which are formed at high temperature, may affect other layers formed previous processes[1]. In contrast, organic gate insulators have low rms roughness and low mismatching of insulator and semiconductor layer. Among those, poly-imide can be a good candidate as a gate insulator because, it has many merits such as a pentacene surface alignment effect by rubbing process, high thermal resistance, high hydrophobic property. In the other hand, VDP process is appropriate for mass production in various end-user applications, because it has the advantages of shadow mask patterning and is an in-situ dry process with flexible low-cost large-area displays. The proposed method could be applied to an in-situ solution-free process to fabricate OTFTs during all fabrication steps. The bottom-contact devices are the only option for a fully lithographic pentacene process. Also, organic semiconductor with high mobility and good molecule ordering, and organic gate dielectric with high breakdown voltage and low leakage current will be adopt to bottom-contact structure. With bottom contacts, the area for carrier transport to the contacts is small, essentially just a line at interface between the channel and the contact since the pentacene will not be accumulated in the regions above the S/D contacts.[2,3]

2. Experimental

OTFTs were fabricated to demonstrate that thermally evaporated polyimide can be used as an adhesion layer. All our devices were fabricated on glass substrates, which was the bottom-contact structure as shown in Figure 1, the 100 nm-thick indium-tin-oxide (ITO) as a gate electrode was sputtered and the 0.2 ㎛-thick SiO_2 as gate insulator was deposited by plasma enhanced chemical vapor deposition (PECVD). To improve the quality of the organic semiconductor /dielectric interface, PI film was co-deposited by VDP process on the SiO_2 as adhesion layer, respectively. Here, PI adhesion layers were formed as different thickness of 15nm, 45nm, 75nm, respectively.

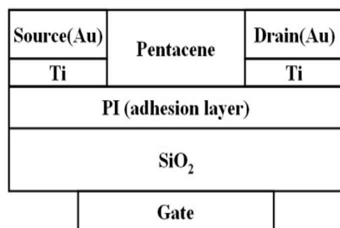


Figure 1. The schemes of OTFTs.

Polyimides are polymers made from the polymerization of an acid dianhydride (6FDA) and a diamine (ODA). They are characterized by the presence of the imide functionality, a cyclic tertiary amine bound by two carbonyl groups, and either an aliphatic or aromatic groups in the main chain. The curing process and the associated link will affect mechanical, thermal, and electrical properties of polyimide. This heat treatment, known as "curing", usually has been done at temperature range of 150~300℃. Figure 2 shows the preparation of polyimide via the condensation of carboxylic dianhydride and dianiline; 6FDA-ODA. In result, we showed Fourier transform infrared (FT-IR) analysis profiles of polyimide.[4] The titanium(Ti) used as adhesion metal layers between gold(Au) used as source/drain(S/D) electrodes and gate insulator was deposited to through shadow mask inside thermal vacuum evaporator. Here, Ti adhesion metal layers were formed as different thickness of 1nm, 2nm, 3nm, 4nm. The drain and source contacts were formed thermal evaporation through a shadow mask to form 40nm thick gold (Au). The fabricated OTFT has a channel length of 50 μm and width of 2. 5mm(W/L=50).

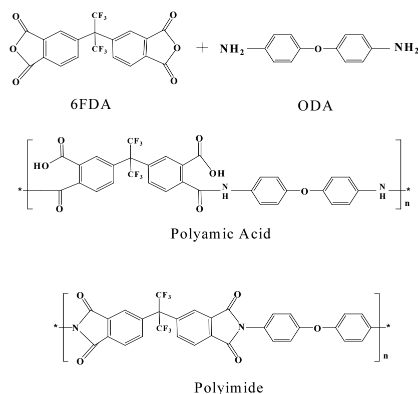


Figure 2. The simplified mechanism of polyimidazation via the condensation of 6FDA and ODA

Pentacene as active layer was deposited by thermal. evaporation at 5×10^{-7} torr, deposition rate of 0.3 Å/s, and total thickness of 60 nm after material purification by vacuum gradient sublimation During the deposition of pentacene, the substrates were held on room temperature. Electrical characteristics of the devices were measured in an air atmosphere using EL421C, semiconductor test and analyzer made by ELECS Co.

3. Results and discussion

OTFT fabricated has a channel length of 50 μm and width 2.5 mm, respectively. OTFT fabricated without treating surface of SiO_2 shows very poor electrical characteristics and flow much leakage currents.

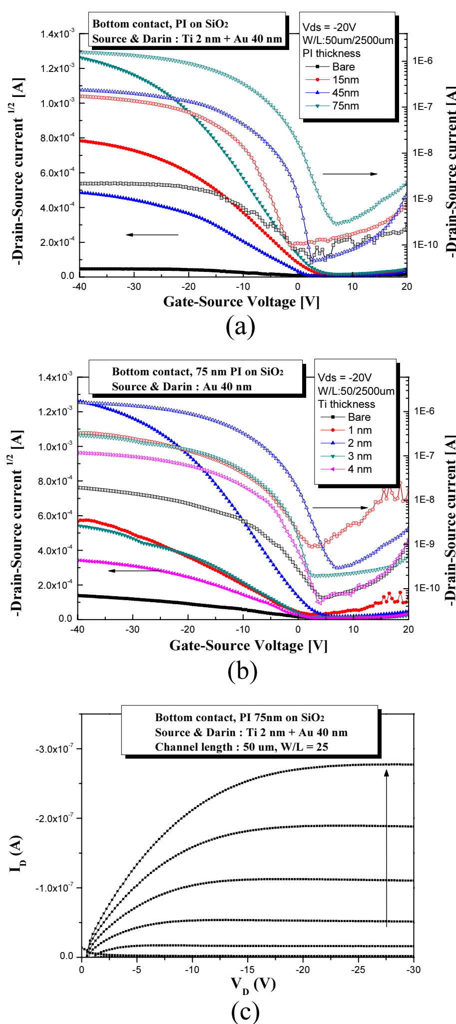
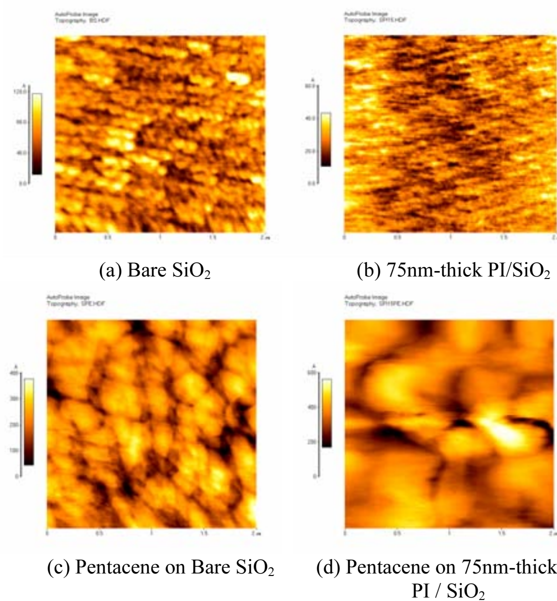


Figure 3. (A) Comparison with electrical transfer characteristics according to PI-thickness. (B) Comparison with electrical transfer characteristics according to Ti-thickness. (C) Output characteristics of OTFTs according to change the gate voltage (0V ~ -30V, step 5V)

As shown in Fig. 3, also, the drain current didn't flow in the channel and flow into gate dielectric because of the disordering pentacene molecules and the interstitial defects in the corner of SiO_2 and source electrode. However, the pentacene OTFT shows typical p-type characteristic and good saturation behavior in the case of applying adhesion layers as shown in Fig. 3. The gate dielectric is a structure which is consist of SiO_2 and polymeric film using as adhesion layer and have the thickness of 200 nm and 75 nm, respectively. Polymeric film plays a role of an adhesion layer to supply smooth surface for pentacene growth.



(a) Bare SiO_2 (b) 75nm-thick PI/SiO_2

(c) Pentacene on Bare SiO_2 (d) Pentacene on 75nm-thick PI / SiO_2

Figure 4. Surface morphologies of pentacene film on the adhesion layer.

Figure. 4. (a) and (b) are a topographic image of SiO_2 surface, respectively and they show an amorphous surface with RMS (root mean square) roughness of 17.4 Å, respectively. In comparison, figure. 4. (c) and (d) are also topographic image of PI surface on SiO_2 and the RMS surface roughness is 5.6 respectively, which means PI adhesion layer considerably reduced the surface roughness on dielectrics. The surface roughness is often induced intentionally to improve adhesion ability between the polyimide and other films and, therefore, such a smooth surface is favorable to obtain higher mobility of organic transistors [5]. Based on these results, we also have investigated the morphology of pentacene films deposited on dielectrics and PI adhesion layer. The morphology of a pentacene films on SiO_2, PI/SiO_2 is shown in figure. 4. (a), (b), (c) and (d). The AFM data in figure. 4. shows that the morphology of pentacene on PI adhesion layer is very different from that on bare insulator substrates. It was found that the crystal grain size on PI polymeric film surface, 1.8~2 μm, was larger than that on bare surface, 0.5~0.7 μm, and the grain boundaries were narrow and dense. In this case, the increase in crystal size seems to be attributed to the reduced roughness of the dielectric.

Table 1. Surface energy of gate dielectrics and PI on dielectrics

Gate dielectric	Contact angle [°]		Polar	Dispersion	Surface tension
	Water	Diiodo methane	[mJm^{-2}][a]	[mJm^{-2}][a]	[mJm^{-2}][a]
SiO_2	28	21.00	31.70	36.82	68.52
SiO_2/PI	76.00	31.00	4.74	40.35	45.09

Dielectrics and PI on dielectrics are listed in Table 1. In case of SiO_2, the PI deposited on dielectric shows the decrease of surface energy and polarity compared with the other one. In case of SiO_2, PI deposited on silicon based dielectric and bare silicon based dielectric, however, show the quite similar surface characteristics. In generally, since the surface of inorganic insulating layers has a hydrophilic property which means a higher polarity and surface energy, it may disturb the growth of pentacene with highly ordered.[6]

Table 2. Comparison of OTFT performances PI & Ti with different thickness on the SiO_2

	On the SiO_2			
Channel length (μm)	50 (W/L=50)			
Ti thickness[nm]	**2nm**			
Pi thickness[nm]	0	15	45	75
Threshold voltage[V]	3.5	3	3.2	1.8
Subthreshold slop [V/decade]	13	5	1.8	2.9
On/Off ratio [A/A]	5×10^{1}	1×10^{3}	5×10^{3}	7×10^{3}
Mobility [Cm^2/Vs]	0.00001	0.0023	0.001	0.01
Off current [A]	3E-10	3E-10	3E-10	3E-10

	On the SiO_2				
Channel length (μm)	50 (W/L=50)				
Ti thickness[nm]	0	1	2	3	4
Pi thickness[nm]	**75nm**				
Threshold voltage[V]	2.3	4.9	1.8	8	3
Subthreshold slop [V/decade]	7	13	2.9	3.2	5
On/Off ratio [A/A]	4×10^{2}	3×10^{2}	7×10^{3}	3×10^{3}	5×10^{3}
Mobility [Cm^2/Vs]	0.0002	0.0001	0.01	0.0012	0.0006
Off current [A]	9E-11	9E-10	3E-10	8E-11	5E-11

Comparison of OTFT performances PI & Ti with different thickness on the SiO_2 are listed in Table 2. The pentacene TFT works in the accumulation enhancement mode. The field-effective mobility is estimated from the slope of a plot of the drain current

($I_D^{1/2}$) versus the gate voltage (V_G). We have obtained a mobility value of about 0.01 cm^2/Vs as saturation mobility. In the transfer characteristic curve shown in Fig. 3, the on-off current ratio ($I_{on/off}$) is about 10^4 in a gate voltage span between 20 and -40 V while the drain voltage (V_D) set at -20 V. I_D and $log(I_D)$ characteristics of OTFTs according to the gate voltage(V_G) is shown figure 3. In the case of bottom-contact configuration, some chemicals are treated onto the source and drain electrodes to improve the contact problem between pentacene and metals. The characteristics of OTFT mentioned above are obtained without the chemical modification of Au source and drain electrodes. Also, poor OTFT stability can result from defects, both in the semiconductor, in the adhesion layer and in the dielectric, as well as at the interfaces between them. In addition, When the thickness of the Ti layer is more than nm, the thickness of the accumulating layer in the pentacene channel is thinner than the thickness of the Ti layer. Because the Ti layer does not make good electric contact with pentacene, carriers have to be injected from the Au layer into the accumulating-channel layer through an insulating region of pentacene. This insulating region would give rise to high series resistance. When the Ti layer is thinner than the accumulating-channel layer, carriers are directly injected into the conduction layer from the Au layer.[7] These results were caused by improvement of quality at interface between semiconductor and dielectric, which may be advanced by inserting PI adhesion layer.

In conclusion, we have performed an experimental and theoretical investigation of the grain size and the energy barrier dependence of the OTFTs electric characteristics.

4. Summary

It was demonstrated in this letter that the molecular ordering of pentacene could be enhanced by PI adhesion layer which has a lower surface energy and roughness than SiO_2. Besides, when the thickness of the Ti layer is more than 2~4 nm, carriers have to be injected from the Au layer into the accumulating-channel layer through an insulating region of pentacene. The OTFTs obtained the on/off ratio of $\sim 10^4$, threshold voltage of 1.8V, subthreshold slop of 2.9 V/decade and field effect mobility about 0.01 cm^2/Vs.

5. Acknowledgements

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