Electrostatic discharge in TFT manufacturing process

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Abstract

Thin Film Transistor (TFT) manufacturing process is complicated. Electrostatic discharge (ESD) occurs during every process step. This paper describes ESD phenomena in terms of TFT design and processing flow. The abnormal contact between equipment and glass is found out to be the key reason causing ESD.

1. Introduction

The aim of array process is to form an array of thin film transistor and pixel on glass. TFT normally includes gate, gate insulator and amorphous silicon (a-Si), source and drain, passivation, translucent pixel electrode (ITO). The cross-sectional view of one pixel and TFT is shown in Fig.1. As other semiconductor devices, ESD occurring during array process destroys device and lead to low production yield. The damage caused by ESD in TFT includes insulator broken down (DGS-data and gate short, DCS-data line and common line short), discontinuous metal line (GO-gate line open, DO-data line open). Three types of ESD defects are shown in Fig.2, 3, and 4 respectively. The FIB (Focus Ion Beam) image in Fig.5 shows the microscopic structure of DGS and DCS. The image reveals that gate insulator and a-Si layer are broken down and gate layer contact data layer directly. SEM image shown in Fig.6 indicates both data line and insulator above the gate line are completely destroyed. ESD defects easily occur in large area. It is difficult to repair at later process, which is detrimental to the production yield. This paper compares the process and design of array substrate and investigates the root cause of ESD, which aims at the solution of ESD in TFT mass production.

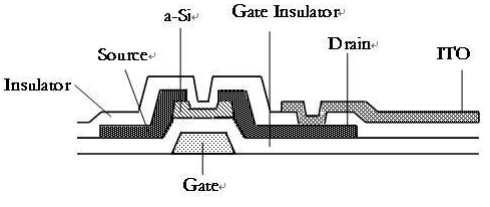

Fig1. TFT pixel structure

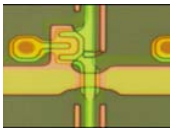

Fig.2. ESD - DGS

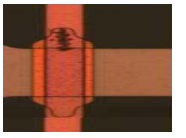

Fig.3.ESD - DCS

Fig.4. ESD – DO

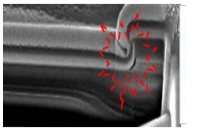

Fig.5. FIB image of insulator broken down

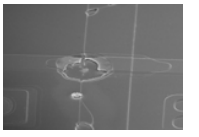

Fig.6. SEM image of metal line open

2. ESD defect analysis

It is well known that the atom is the base particulate of substance. An atom consists of atomic nucleus made of positron and electronegative electron. Generally an unstable atom causes static charges. Usually the positron and electron is equal in an atom. When the substance under the exterior impact such as contact, extrusion, heating and etc. lose or get electrons, the charge balance in atom is broken. It leads the substance to be electriferous. Static is formed if the electrons can not move. When the static charges build up to some extent, discharge occurs to release the energy release by lightening and heat.

The analysis demonstrates that the position of ESD defects perfectly match with abnormal contact area of some equipment pins. When the glasses contact with the pins of the equipments, the electrons transport from the glass to equipment and the static charges are produced. The symplectic electron layers are formed between them as shown in Fig.7. If the static charges can not neutralize or dissipate, different polarity charges assemble on pin and glass. When the static charges accumulate to critical broken down density (Q^{+}_{BD}), ESD occurs [1].

$$Q^{+}_{BD} = \frac{e\alpha_0 t_{ox}\left(1-\frac{1}{e^{\tau}}\right)}{\sigma e^{1/E}} \quad (1\text{-}1)$$

$$E = \frac{\sigma}{\varepsilon_0} \quad (1\text{-}2)$$

$$E = \frac{U}{d} \quad (1\text{-}3)$$

The abnormal contacts cause the defect area static density higher than normal area as shown in Fig.8.

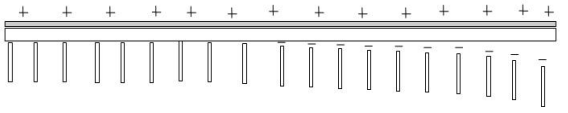

Fig7. Static distributing on glass and equipment

Fig8. Static distributing on abnormal contact

Table1. DGS defect ratio Vs Design

Model	Design-1	Design-2
DGS defect Ratio	1.53%	0.09%

ESD-DGS defects occur when TFT's insulator is broken down and cause data and gate contact directly. Because gate layer metal contact glass surface directly, most of static charges accumulate on gate pattern. Table 1 reveals the different ESD-DGS defect ratio between two array designs shown in Fig.9 and 10. The gate pattern includes gate scan line and shield bar. The shield bar of design 1 is isolated stick-shape. The shield bar of design 2 is connected to each other forming the shape of "H". The distance d between shield bar and gate scan line of design 2 is farther than that of design 1. When the density of static charges σ increases at the abnormal contact area, the H type shield bars disperse static charges to the lower static charges density area right away, and the electric field intensity E between shield bar and Gate scan line reduce. According to the formula 1-1, 1-2, 1-3, the Q+BD of deign 2 is higher than design 1. Therefore the DGS defect ratio is lower.

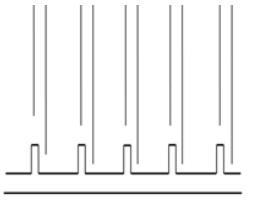

Fig.9. Gate pattern: design 1

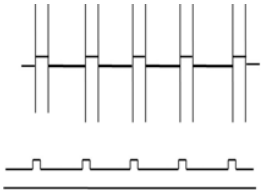

Fig.10. Gate pattern: design 2

ESD-DCS defect occur when TFT's insulator is broken down and cause data and common line contact directly. The DCS defect occurs at the cross section of data line and common line made of gate metal. The junction curvature affects the occurrence of ESD [2]. When a-Si diffuse to insulator forming p-n kink on both flank surface and lower surface, the p-n kink's flank is cucumiform and lower surface is flat. At the head of a-Si island, the p-n kink is spherical surface [3]. The Fig.11 shows that the break down voltage of flank surface and spherical surface is lower than under surface. ESD occurs at the under surface and spherical surface. When the inductive electron density grows to Q^{+}_{BD}, ESD occurs.

The defect ratio is different in different processes as shown in Table 2. For 4 mask processing technology, one exposure step is adopted to form active layer (gate insulator and a-Si layer) and data line layer. For 5 mask processing technology, two exposure steps are adopted to form active layer and data line layer respectively. The shape of active layer is different as shown in Fig.12, 13. 4 mask processing technology forms a-Si under all parts of data line. 5 mask processing technology forms isolated a-Si island between common line and Data line. The accumulation of static charges on common line builds up the electric field between common line and a-Si. Because of a-Si island shape in 5 mask processing technology, the inductive electron can not be released. For 4 Mask processing technology, inductive electrons can release to the area of lower density. Inductive electron density unlikely goes up to Q^{+}_{BD}, and ESD is not easy occurring at the cross section area.

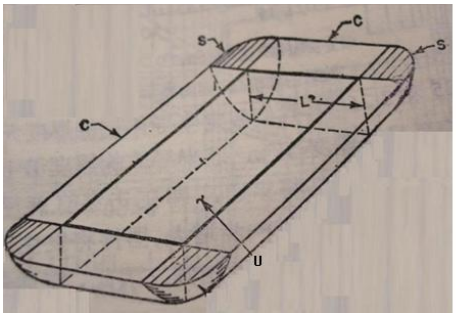

Fig11. Data and common section construction (C: cucumiform S: spherical U: under)

Table1. DCS defect ratio Vs Process

Process	5 mask	4 mask
DCS defect Ratio	1.81%	0.07%

Fig.12.Data– Common structure : 5 mask

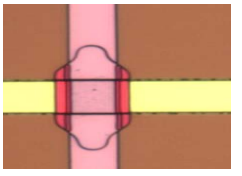

Fig.13. Data – Common structure: 4 mask

The Fig.4 shows ESD-DO defect. SEM image indicates both data line and insulator on the data line are totally attacked. This defect is caused by some equipment abnormal contacts with ITO metal layer during ITO exposure process. The ESD occurs at the cross section of common line and data line because of the high curvature and Q^{+}_{BD}. The defect ratio is different for different insulator thickness. The relationship between thickness and defect ratio is shown in Fig.14. According to formula (1-1), the relationship of insulator thickness and critical electron density (Q^{+}_{BD}) is directly proportional. The ESD defect ratio is almost 0.0% when the insulator thickness reaches 3500Å.

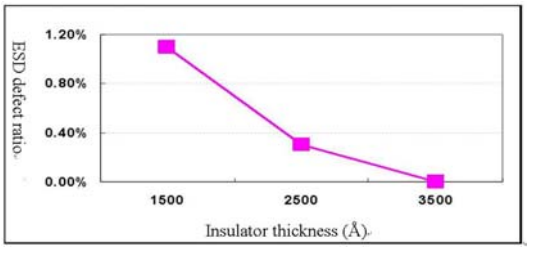

Fig.14 ESD ration Vs Insulator thickness

3. Conclusions

The abnormal contacts between glass and equipment cause higher partial static density, leading to ESD defects. Design pattern, processing technology and insulator thickness heavily impact TFT`s immunity to ESD damage.

4. Acknowledgements

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