Study of surface state density of hydrogenated amorphous silicon thin-film transistors by admittance spectroscopy

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Abstract

We reported a simplified circuit model to investigate the interface states and the quality of a-Si film based on a MIS structure using admittance spectroscopy. The model can be employed easily to monitor the fabrication process of thin-film transistor and to obtain the important parameters.

1. Introduction

Recently, hydrogenated amorphous silicon (a-Si:H) is applied in numerous applications, especially in thin-film transistors (TFTs).[1] The performance of a-Si:H TFTs is well know to depend strongly on the fabrication process such as gas dilution, and on the substrate temperature, pressure and RF power during film deposition.[2-4] A method for monitoring the fabrication process must be developed to elucidate the effects of these process conditions. Over the past years, capacitance-voltage (*C-V*) measurements have been a powerful diagnostic tool in studying the electrical properties and in monitoring the fabrication processes of metal-oxide-semiconductor (MOS) structures.[5] However, *C-V* measurements of metal-insulator-a-Si:H (MIS) are limited because of the high density of defect states and the low electron and hole mobilities of a-Si:H layer.[6] Obtaining information by *C-V* measurements directly at various frequencies and temperatures is difficult, especially under depletion operating condition, because numerous factors simultaneously govern the frequency response of capacitance; these factors include the interface states, the deep buck trap state, lateral current flow and others. Accordingly, admittance spectroscopy is an exact method that uses a correct equivalent circuit model to investigate the MIS structure along with an alternative direct measurement method. Several works have involved *C-V* measurements on MIAS, a-Si:H Schottky diode, and TFTs structures.[7,8] However, systematic study of capacitance-frequency (*C-F*) and conduction/frequency-frequency (*G/F-F*) measurements of an MIAS structure are few. In this study, temperature-dependent admittance spectroscopy was employed to investigate the interface states and the properties of a-Si:H film. Careful and detailed *C-F* and *G/F-F* measurements of the MIAS configuration were made

2. Experimental

Two conventional inverted-staggered MIS capacitors were fabricated to be studied by admittance spectroscopy. The SiN_X layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) with a mixture of H_2, NH_3, N_2 and SiH_4 gases at 1.2 torr for both devices A and B. The a-Si:H was deposited on top of the SiN_X film from a glow discharge of pure SiH_4 at 0.7 torr with a substrate temperature of 270℃ and an RF power density of 70 mW/cm^2. The a-Si:H film was slightly n-type with different H_2 dilutions of SiH_4. The H_2/SiH_4 ratios of device A and B were 1250/250 and 2500/250, respectively. Another phosphorus doped (n^+) a-Si:H layer was deposited on top of a-Si:H to ensure ohmic source or drain contact. The thicknesses of the SiN_X, a-Si:H, and n^+ contact layers were 330, 200, and 50 nm respectively. The areas of the MIS capacitors were both 500×1000 μm^2. Aluminum was used as both gate and source/drain metallurgy. Two a-Si:H TFTs devices with a W/L ratio of 15 μm / 3 μm were also fabricated, in which all of the thin films were deposited under the same process conditions as devices A and B. The MIS and TFTs were fabricated using standard photolithographic techniques. Table 1 presents the extracted parameters of both devices under V_{DS}=5 V.

TABLE 1. Extracted parameters of a-Si:H TFT s for device A and B under V_{DS}=5 V

Device	Swing (V/dec)	Mobility (cm^2/V-s)	I_{ON} (A) (Vg=20V)
Device A	0.8	0.81	3.30×10^{-6}
Device B	0.58	1.11	5.73×10^{-6}

3. Results and discussion

An equivalent circuit model must be developed for admittance spectroscopy measurement. The schematic band diagram of the MIS capacitor in Fig. 1 (a) for a slightly doped n-type a-Si:H under electron depletion condition elucidates the physics of the MIS capacitor. In the MIS capacitor, a highly resistive intrinsic a-Si:H is used. Therefore, the a-Si:H bulk capacitance and resistance have to be considered in the equivalent circuit model. Based on the properties of a-Si:H, an circuit model was show in the Figs. 1(b) for depletion. C_{SiN} represents the geometric capacitance of the insulator layer (SiN_X), and $C_{a\text{-}Si}$ and $R_{a\text{-}Si}$ are the geometric capacitance and resistance of a-Si:H, respectively. C_D and R_D represent the capacitance and resistance of depletion, respectively. C_S and R_S are the interface state capacitance and the specific emission time constant of charge trapped in the interface state, respectively. In the model, the $C_{a\text{-}Si}$ and C_D are introduced. The values of $C_{a\text{-}Si}$ and C_D are determined by the width of space charge region. In depletion conditions, $R_{a\text{-}Si}$ should dependent linearly on the difference between the total a-Si:H film thickness and the width of the space charge region. In depletion, therefore, the equations for $C_{a\text{-}Si}$, $R_{a\text{-}Si}$ and C_D are

$$C_{a-Si} = \varepsilon_r \varepsilon_0 A/(D-W)$$

$$R_{a-Si} = \rho(D-W)/A$$

$$C_D = \varepsilon_r \varepsilon_0 A/W$$

where D is the total a-Si:H film thickness; W represents the width of the space charge region, ε_r and ε_0 represent the dielectric constant of aSi:H and the permittivity of free space, respectively, ρ is the resistivity of a-Si:H film, and A is the active area of the MIS device. In the depletion, C_S should be considered in the equivalent circuit model because the number of interface trapped charges is comparable to the number of mobile charges in the a-Si:H film. However, the effect of deep-level trapped charges or generation-recombination charges can be ignored herein because its response frequency is approximately 0.1 Hz at room temperature which significantly exceeds the limit of the equipment. Hence, C_S is in parallel with C_D, and can be determined in depletion by C-F measurement using the equivalent circuit model. Consequently, the ac parallel equivalent capacitance of the equivalent circuit model in Fig. 1(b) is given by:

$$C(\omega) = \frac{C_{a-Si}C_1}{C_{a-Si}+C_1}\left[1+\frac{C_1/C_{a-Si}}{1+\omega^2 R_{a-Si}^2 (C_{a-Si}+C_1)^2}\right]$$

where

$$C_1 = \frac{C_{SiN}C_P}{C_{SiN}+C_P}$$

$$C_P = C_D + \frac{C_S}{1+\omega^2 {R_S}^2 {C_S}^2}$$

$$C_S = qN_S$$

where q is the electronic charge, and N_S is the density of interface states. The above equations indicate that capacitance depends strongly on the frequency under the depletion operating conditions, which fact can be used to study the properties of a-Si:H and the density of interface states by admittance spectroscopy.

Figures 2 (a) and (b) show the *RT C-F* and *G/F-F* spectra, respectively for different gate biases applied to the MIS capacitor. As the bias is increased beyond -1 V, the operating condition enters the depletion region and the capacitance increases rapidly at low frequency region due to the decrease of *W*. During depletion (-1 V~2 V), the *C-F* spectra show two drops at the inflexion frequencies of 10K Hz and 200K Hz of equal to the inverse *RC* time constant of the interface states and the a-Si:H film, respectively. In *G/F-F* spectra, the peaks are associated with the inflexion frequencies. Therefore, the inflexion frequency can be more clearly observed in Fig. 2 (b). Figures 3 (a) and (b) plot the simulated ac parallel equivalent capacitance under depletion operating conditions, obtained using the above equations, for devices A and B, respectively. Fig. 3 (a) and (b) show excellent agreement between simulated (open squares) and experimental (solid curve) *C-F* spectra for devices A and B, respectively. The density of interface states and the resistance of a-Si:H at various *Vg* can be determined from fitted data in Figs. 3 (a) and (b). Figure 4 (a) polts the interface states density as a function of *Vg* for device A and B in the depletion. The values of density of interface states for both devices, obtained from Fig. 3 are comparable to those obtained by others using other methods.[9] Under the same gate bias, the density of interface states of device A always exceeds that of device B which fact explains the lower swing observed in device B. Fig. 4 (b) plots $R_{a\text{-}Si}$ as a function of thickness of a-Si:H in depletion region. From Fig. 4 (b), $R_{a\text{-}Si}$ is proportional to the difference between *D* and *W*, indicating the correctness of the equivalent circuit model. Furthermore, the resistivity of a-Si:H can be also determined. The resisvities of device A and device B are 3.48×10^6 and 1.16×10^6 Ω-cm, respectively.

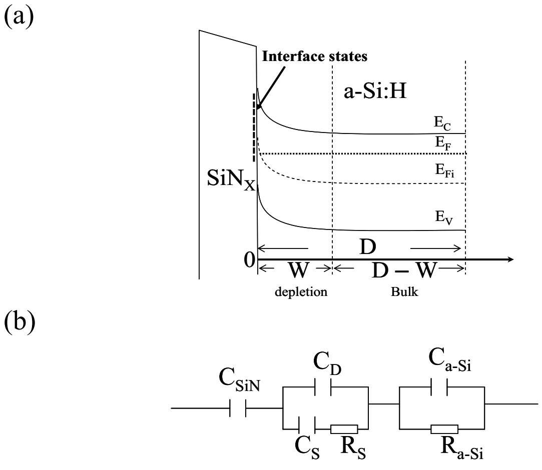

FIG. 1. The band diagram and equivalent circuit models of MIAS structure under depletion.

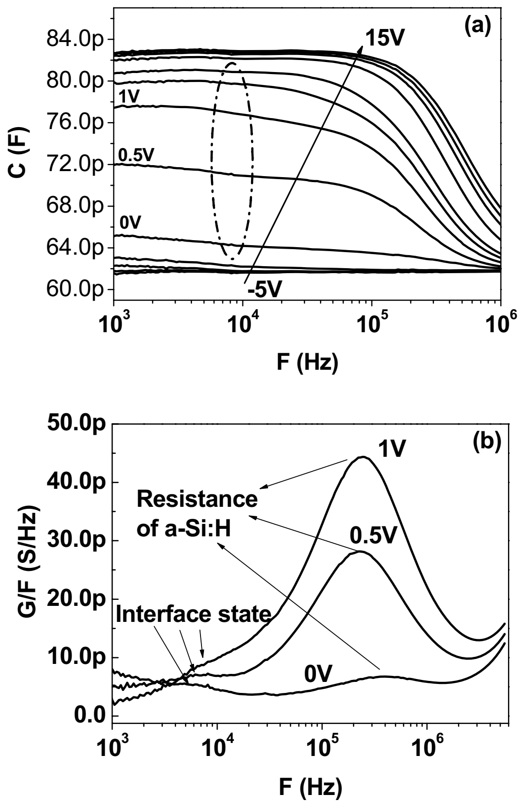

FIG. 2. A admittance Spectroscopy spectra on the MIAS structure for device A.

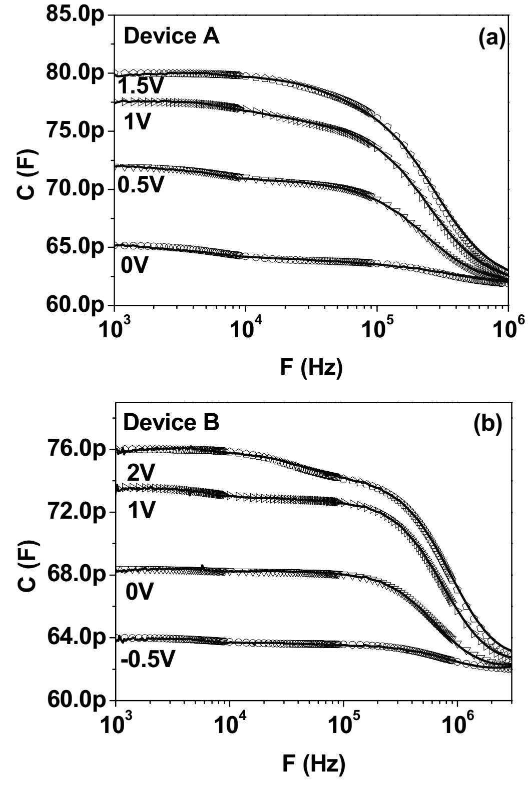

FIG. 3. Simulations (open squares) and experiments (solid curve) of *C-F* curves in depletion region. (a)device A, (b) device B.

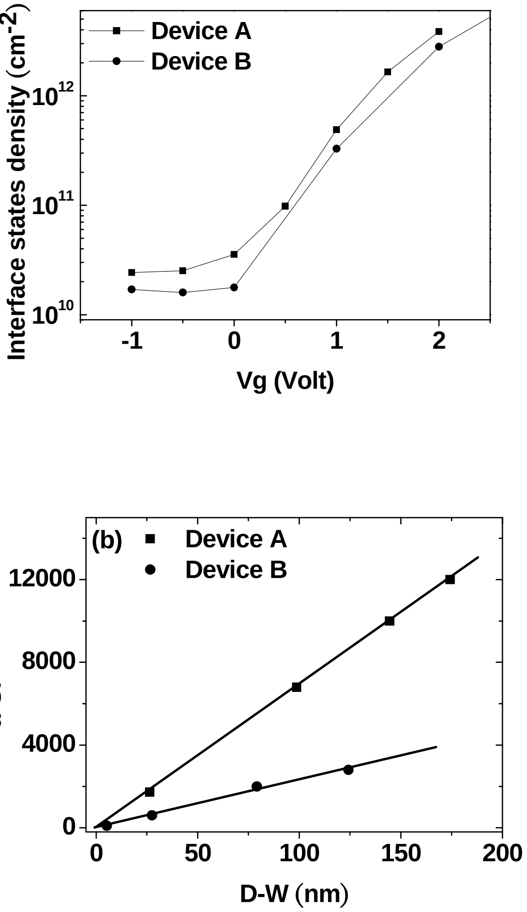

FIG. 4(a). Comparison of density of interface states at various gate bias between device A and device B. (b) Ra-Si as a function of thickness of a-Si:H in depletion region for device A and device B. The resistances and depleted widths are derived from fitted data using the equations of ac parallel equivalent capacitance.

4. Conclusions

Based on the properties of a-Si:H, the equivalent circuit model was developed and simplified for depletion operating conditions. Excellent agreement between the experimental data and the proposed equivalent circuit models was found. The simulation *C-F* measurement using equivalent circuit models easily yielded the interface density of states at room temperature. The resisvity of a-Si:H film was also determined to evaluate the quality of the a-Si:H film. Experimental data concerning the MIS structure agreed excellently with the output characteristics of TFTs devices. Consequently, admittance spectroscopy measurement based on the equivalent circuit model can be used as a powerful and efficient tool for the process monitoring of TFT devices.

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