# Low-Temperature Processable Polyimide Gate Insulator and Hybridization Approach for High Performance Pentacene Thin Film Transistor

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## Abstract

*We have synthesized a novel fully soluble and low-temperature processable polyimide gate insulator (KSPI) through one-step condensation polymerization. For the preparation of KSPI, 5-(2,5-dioxytetrahydrofuryl)-3-methly-3-cyclohexene-1,2-dicarboxylic anhydride (DOCDA) and 4,4-diaminodiphenylmethane (MDA) were used as monomers and fully imidized KSPI was completely soluble in organic solvents like γ-butyrolactone and 2-butoxyethanol, etc.*

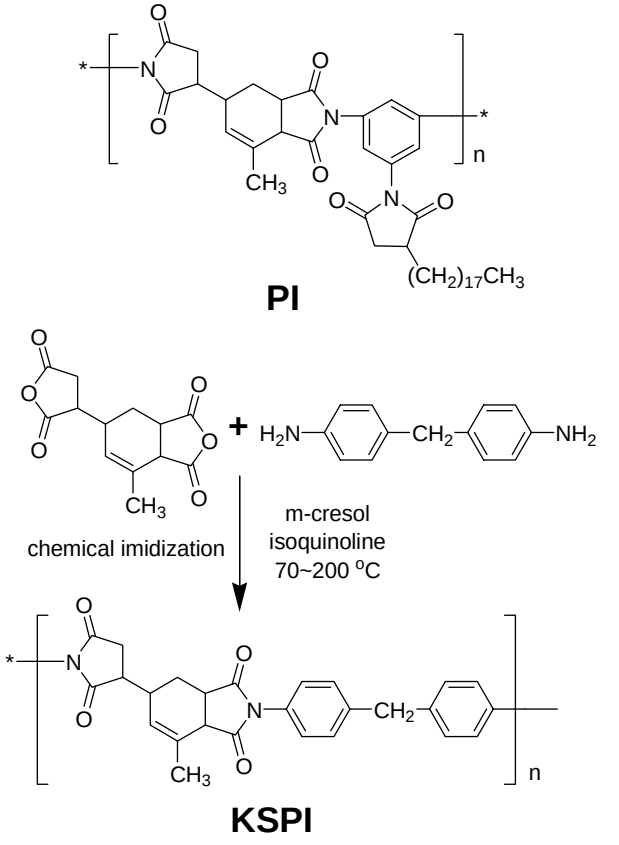
## 1. Introduction

Flexible organic electronics enabled by organic thin film transistor (OTFT) devices has received much attention of late due to the potential of this technology to impact smart card, radio frequency identification (RFID) tags, nonvolatile memories, sensors and driver circuits in flexible display [1-4]. The major new advantage of organic materials when incorporated into electronic devices is the possibility of fabricating mechanically flexible devices on flexible substrates. However, in order for this so called, flexible technology to move forward, flexible gate dielectric materials must be developed and the performance of such devices must be optimized. But most of studies of organic TFTs employed silicon dioxide/heavily doped silicon as the insulator/gate pair. To realize flexible organic electronics, not only organic semiconductor but also all other components of TFT should be replaced by organic materials. Therefore there are increasing interests on polymeric materials as gate dielectric materials in OTFT. Several polymeric gate dielectrics, such as poly(vinyl phenol) (PVP), poly(methyl methacrylate) (PMMA), poly(vinyl alcohol) (PVA), benzocyclobutene (BCB), and polyimide (PI), have been investigated [5,6]. Among them, PIs are currently considered as promising candidate as a gate dielectric because of their good chemical resistance and mechanical property. But one of the big obstacles of PI materials to be solved is high processing temperature. Recently we have reported a unique surface modification method of PI gate dielectric by hybridization tool [7]. But in that case PI gate dielectric should be thermally treated at 230 $^{o}$C to make thin film in OTFT. Such high processing temperature could not be applied for the flexible organic electronics application. In this work, we present synthesis of new low temperature processable polyimide can be processed into thin film at 150 $^{o}$C for gate insulator and hybridization approach of gate insulator to obtain high performance pentacene thin film transistor.

## 2. Experimental

4,4-Diaminodiphenylmethane (MDA) was purchased from Mitsubishi Kasei Chemical Co. (Japan) and 5-(2,5-dioxytetrahydrofuryl)-3-methly-3-cyclohexene-1,2-dicarboxylic anhydride (DOCDA) from TCI Chemical Co. (Japan), and dried at 100 $^{o}$C for 24 h in a vacuum oven prior to use. KSPI was synthesized by condensation polymerization using isoquinoline as a catalyst in m-cresol. The synthesis of PI was reported previously in our group [7] and was prepared as same manner in literature. *m*-Cresol, which was received from Junsei Chemical Co. (Japan) was used without further purification. Isoquinoline was purchased from Aldrich Chemical. Co. and used as received. All other chemicals used for the synthesis and purification of monomer and polymer were also commercially available and were used without any further purification. Pentacene (98% purity) was

selected as the active layer in this study, and was purchased from Aldrich Chemical Co. and used also without any further purification. Synthetic scheme and chemical structure are shown in Scheme 1.




**Scheme 1**. Chemical structure and synthetic scheme of PI and KSPI.

The OTFT device geometry for all electrical characterizations was a top-contact. Indium tin oxide (ITO) coated glass was used for a substrate and the ITO was patterned (2mm wide stripes) for the formation of gate electrode by a conventional photolithographic method: photoresist coating, ultraviolet light exposure, developing and etching. The patterned ITO substrate was cleaned using the general cleaning process for electronic applications; sonication in detergent, deionized water, acetone and isopropanol in that order for 20 min at room temperature. Polyimide solution (KSPI) was made in γ -butyrolactone and 2-butoxyethanol co-solvent as 8 wt% concentration. In addition, blended polyimide solution (KSPI/PI=98/2, BPI) was prepared in same co-solvent and concentration. KSPI and blended BPI solutions were spin coated on top of the gate electrodes as a gate insulator and then the film was annealed at 90 °C for 10 min and 150 °C for 30 min. The final thickness of the polyimide gate insulator was adjusted about 300 nm. A 60-nm-thick layer of pentacene was deposited on top of the gate insulator through a shadow mask by thermal evaporation at a pressure $1X10^{-6}$ torr. The evaporation rate of the pentacene was 1 Å/s and the substrate temperature was 90 °C. OTFTs were then completed by thermal evaporating a 50-nm-thick source and drain gold electrodes on top of the pentacene layer through a shadow mask, thus created transistor with channel length ($L$) and width ($W$) as 50 and 1000 μm, respectively.

To determine the capacitance and gate leakage of soluble and blended polyimide gate insulators, MIM (metal-insulator-metal) capacitor structures were prepared on the patterned ITO coated glass substrates. Fully soluble KSPI and BPI were spin coated on top of the bottom ITO electrode and then the film was annealed at 90 °C for 10 min and 150 °C for 30 min. MIM devices were then completed by evaporating the top gold electrodes. The final thicknesses of all films were controlled to 300 nm. The active area of MIM device was 50.24 $mm^2$.

## 3. Results and discussion

To investigate capacitance and leakage current properties of KSPI polyimide film, we have prepared a metal-insulator-metal (MIM) device on a pre-cleaned ITO glass substrate by inserting the polyimide layer between the ITO as a bottom electrode and gold as a top electrode. The leakage current density of the device with KSPI was less than $7X10^{-10}A/cm^2$, while biased from 0 to 50 V. The breakdown voltage and the capacitance were measured as more than 2 MV/cm and 88.4 $pF/mm^2$, respectively. Hybridized gate insulator BPI (KSPI/PI=98/2) also showed similar leakage current, breakage down voltage and capacitance (90.2 $pF/mm^2$). We also investigated surface properties of KSPI and BPI insulator. Atomic force microscopy (AFM) images showed similar root-mean-square roughness of both films as 0.28~0.39 nm. However, water contact angle and surface tension of KSPI and BPI were somewhat different, as we expected. The surface tensions of KSPI and BPI calculated from the contact angle of water and diiodomethane were 56.26 and 44.00 dyne/cm, respectively. The contact angle of water on BPI was larger than that on KSPI. This means that the surface of BPI is more hydrophobic by blending KSPI with PI having long alkyl chain as a side chain. Electrical and

surface properties of both insulators are summarized in Table 1.

**Table 1**. Electrical and surface properties of KSPI and BPI.

| | C*i* (pF/mm$^2$) (10KHz) | Dielectric constant (10kHz) | Surface roughness (nm) | Surface tension (dyne/cm) |
|---|---|---|---|---|
| KSPI | 88.4 | 3.63 | 0.28 | 56.26 |
| BPI | 90.2 | 3.99 | 0.39 | 44.00 |

AFM and x-ray diffraction (XRD) experiments were performed in order to investigate the effect of the surface property on the morphology development of pentacene on the gate insulator. Figure 1 show AFM images of 60 nm thick pentacene on the gate insulators. The pentacene on KSPI show a dendritic structure and its grain size is around 0.5~1.0 μm and corresponding XRD pattern (not shown here) is composed of a series of (00*l*) sharp peak indicating that pentacene is highly ordered. On the other hand, pentacene on BPI did not show large dendritic structure and its grain size was somewhat reduced. The main XRD peaks of BPI were observed from the thin film phase (5.71 $^{o}$), and a peak from the bulk phase (6.07 $^{o}$) was also observed. The measured Bragg refraction angle of (6.07 $^{o}$) represents a tilting of the pentacene molecule to the surface of 25.6, indicating that some of the pentacene molecules on BPI are more tilted and possibly contribute to the increase of adhesion on the BPI film.

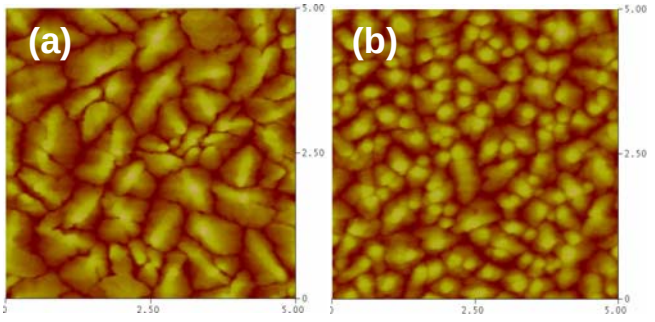



**Fig. 1.** AFM images (5 μm × 5 μm) of pentacene (60 nm) on the (a) KSPI and (b) BPI.

The increased adhesion gives a positive effect on the initial growth mechanism of pentacene on the BPI gate insulator. This leads to the formation of a more stable interface and contributes to the performance improvement of OTFTs. Similar results were reported by several groups [8,9].

Figure 2 show the output ($I_{ds}$ vs $V_{ds}$) characteristics of the OTFT having KSPI and BPI as insulators. The OTFTs exhibit typical p-type characteristics with a clear transition from linear to saturation behavior in both devices. At a given negative gate voltage ($V_{gs}$), $I_{ds}$ initially increases linearly with a small negative $V_{ds}$ and then saturates due to a pinch off of the accumulation layer.

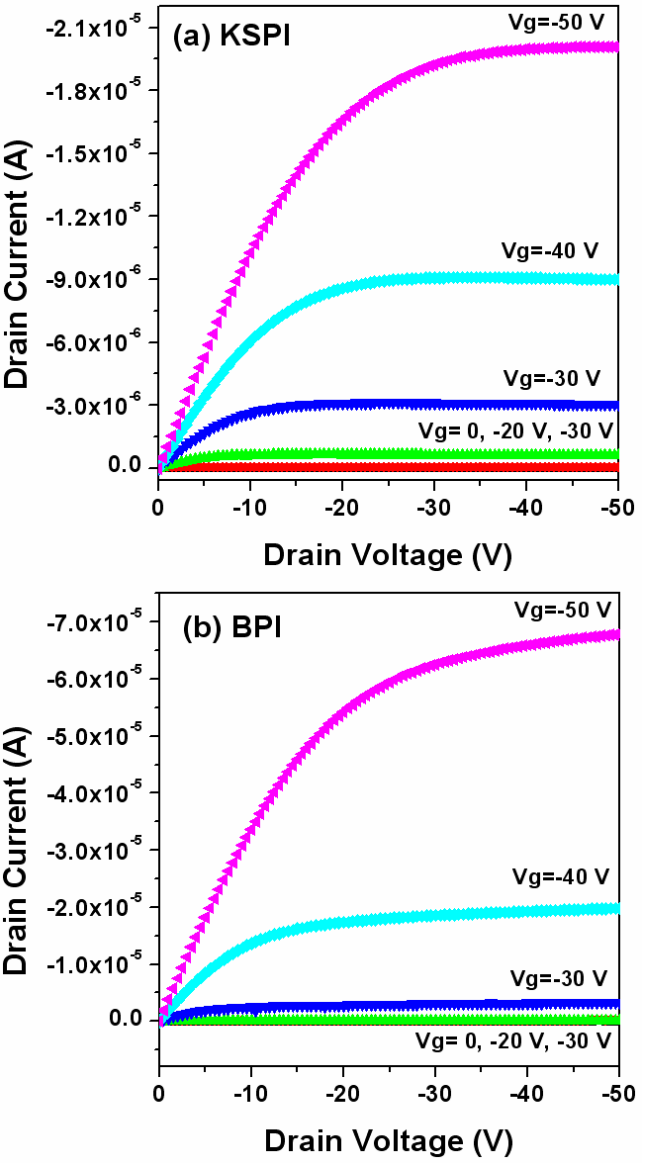



**Fig. 2**. Output characteristics (for drain current vs. drain voltage, $I_{ds}$ vs $V_{ds}$) of OTFTs with (a) KSPI and (b) BPI.

As the negative gate voltage ($V_{gs}$) increases, the device fabricated from BPI insulator exhibits much higher $I_{ds}$ than the device having KSPI as a gate insulator.

Transfer ($I_{ds}$ vs $V_{gs}$) characteristic curves of the OTFT fabricated with KSPI and BPI are shown in Figure 3. The field-effect mobility ($\mu$) was calculated from the plot of the square root of the drain current ($I_{ds}^{1/2}$) and gate voltage ($V_{gs}$) in the saturation regime. The threshold voltage ($V_T$) of the device was determined from the plot of ($I_{ds}^{1/2}$) and $V_{gs}$ by an extrapolating the measured data to $I_{ds} = 0$. When $V_{gs}$ was swept from +20 to -50 $V$ and $V_{ds}$ was set at -40 $V$, the μ, off current, and subthreshold swing (SS) of the pentacene OTFT with KSPI gate insulator were 0.22 $cm^2/Vs$, $2.2 \times 10^{-10}$ A, and 3.8 V/dec, respectively.

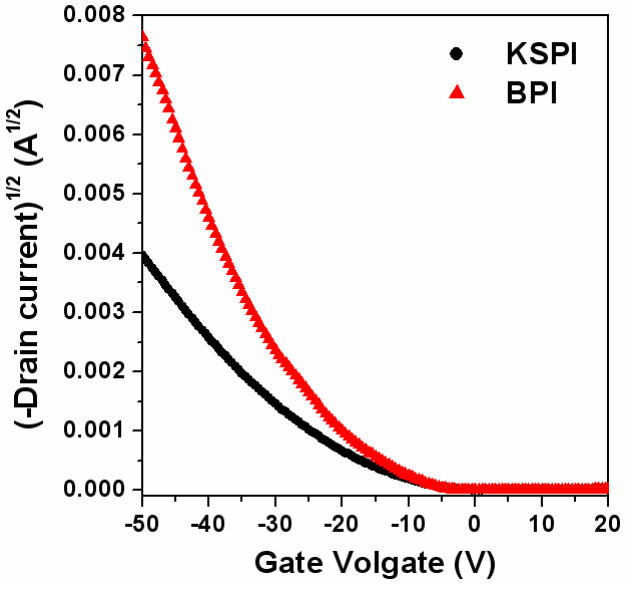



**Fig. 3.** Transfer characteristics (for the square root of the drain current vs. gate voltage, $I_{ds}^{1/2}$ vs $V_{gs}$) of OTFTs with KSPI and BPI.

It is interesting that when blended gate insulator (BPI) instead of KSPI, is used as a gate insulator, the mobility increases by about four times (0.92 $cm^2/Vs$) in spite of the fact that the crystal size of pentacene on BPI is smaller as compared to that of pentacene on KSPI. The performance of OTFTs can be affected by grain size, orientation, and crystallinity of an organic semiconductor. These properties are usually determined by the surface property of a gate insulator, the evaporation rate of a semiconductor, the substrate temperature, and the annealing process, etc.

Considering only the grain size of the pentacene, a decrease in the grain size (increasing grain boundary density) reduces the carrier mobility of OTFTs. This in contrast to our results and some reports form other groups that state that the grain size of pentacene is smaller on surface modified gate insulators with a non polar side chain having insulator than non-blended gate insulator although the performance of OTFTs with blended gate insulator was found to be better. Therefore we conclude that surface property of the gate insulator adds another parameter, which has a dramatic effect on the interface formation between the gate insulator and the semiconductor by altering the initial growth mechanism of pentacene.

## 4. Summary

We have prepared low-temperature processable polyimide gate insulator showing good electrical properties such as a high breakdown voltage and low leakage current. The polyimide as a completely imidized structure exhibited excellent thermal stability, good chemical resistance for common organic solvents as well as low temperature processability. We also have successfully fabricated pentacene OTFTs using polyimide insulator. By employing the gate insulator hybridization method, we got the high performance pentacene TFT and this approach provides a potential design improvement concept for organic insulators for OTFTs.

## 5. References

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