Hardware architecture of a wavelet based multiple line addressing driving system for passive matrix displays

San Lam[*] and Herbert De Smet [*,]**

[*]Ghent University, department ELIS (TFCG Microsystems), Gent, Belgium

TEL:+32-9-2645355, sanlam@elis.ugent.be

TEL:+32-9-2645363, Herbert.DeSmet@elis.ugent.be.

[**]IMEC vzw, division INTEC, Gent, Belgium

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Abstract

A hardware architecture is presented of a wavelet based multiple line addressing driving scheme for passive matrix displays using the FPGA (Field Programmable Gate Arrays), which will be integrated in the scalable video coding architecture[1]. The incoming compressed video data stream will then directly be transformed to the required column voltages by the hardware architecture without the need of employing the video decompression.

1. Objectives and Background

The idea of integration of the scalable video coding architecture with the wavelet based passive matrix display addressing architecture saves the computation of an IDWT (Inverse Discrete Wavelet Transform) for each video frame [1]. Hence it reduces the power consumption of portable devices. The input video frame $B_{video,i}$ of the scalable video decoder enters the FPGA, where a matrix multiplication is performed with the matrix $(F_n^T)^{-1}$according to equation (1), to obtain the column voltage matrix $G_{video,i}$.

$$\mathbf{G}_{\mathbf{video,i}} = \mathbf{cB}_{\mathbf{video,i}} (\mathbf{F}_{\mathbf{n}}^{\mathbf{T}})^{\mathbf{-1}} \quad (1)$$

The analysis matrix F_n is composed of symmetric bi-orthogonal 9/7 wavelet coefficients[2] of dimension n*n, where c is the scaling factor. A necessary condition to calculate the correct column voltages is that the decoded wavelet video frame $B_{video,i}$ needs to be equal to the encoded one given by equation (2). The matrix X_i is the original video frame i and the matrix F_m, the analysis matrix composed of symmetric bi-orthogonal 9/7 wavelet coefficients of size m*m.

$$\mathbf{B}_{\mathbf{video,i}} = \mathbf{F}_{\mathbf{m}} \mathbf{X}_{\mathbf{i}} (\mathbf{F}_{\mathbf{n}}^{\mathbf{T}})^{\mathbf{-1}} \quad (2)$$

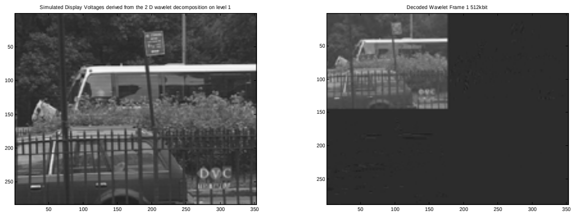

Figure 1. Left the simulated wavelet based driven display voltages using column signals calculated from the 2-D wavelet transformed image B on decomposition level 1. Right: The received quantized 2-D wavelet transformed image frames $B_{video,i}$ .of decomposition level 1.

The obtained simulated display voltages are shown in Figure 1 Left and are obtained by using the column signals calculated from the compressed video frame $B_{video,i}$ shown in Figure 1 Right.

The objective of this paper is to describe a hardware implementation of this proposed integrated system architecture by using the FPGA (Field Programmable Gate Arrays) of Xilinx. The use of FPGA maintains the advantages of the custom functionality of VLSI ASIC devices, while avoiding the high development costs and the inability to make design modifications after production. Furthermore, FPGAs inherit design flexibility and adaptability of software implementations. The approach of design of the integrated architecture was used by a MatLab/Simulink interface instead of the VHDL compiler tool. This approach is gaining much more successful because of the large MatLab programmers of over 1 million world-wide [2].

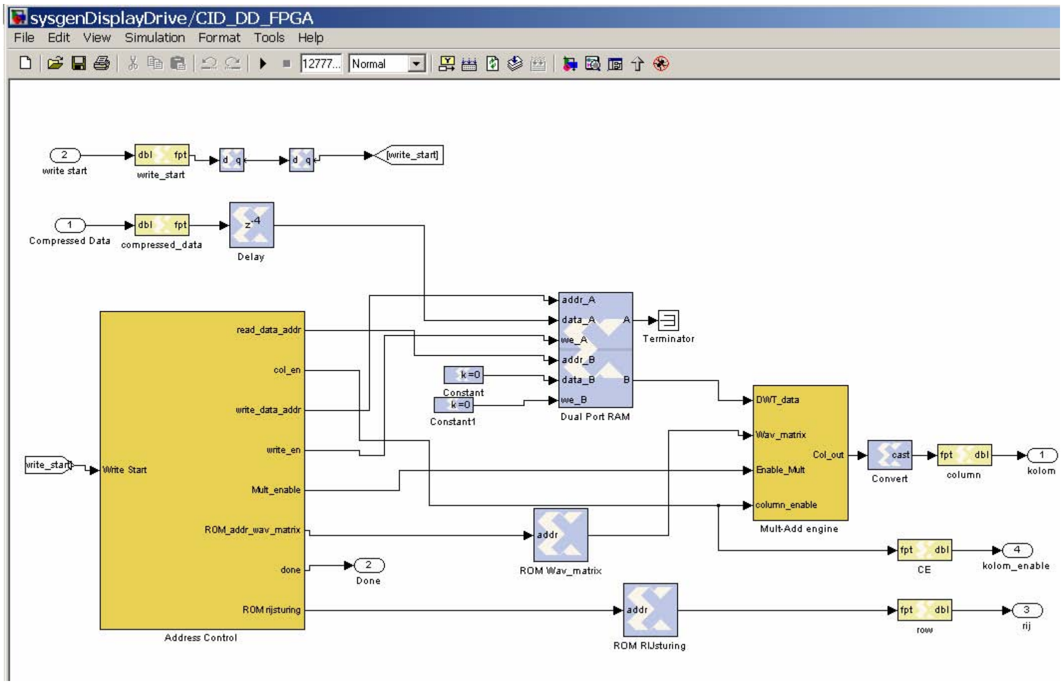

Figure 2. Detailed hardware architecture of the FPGA.

2. Hardware Architecture

A block diagram of the FPGA is shown in Figure 2 which is designed to generate the required column and row signals for driving a passive matrix display of 96*110 pixels. The design is done with the MatLab/Simulink software in combination with the Xilinx System Generator software [3]. The Xilinx Gateway In and Gateway Out blocks provide an interface to the Xilinx Blockset in Simulink. The Xilinx Gateway In block represents an input port into the FPGA, while the Gateway Out block represents the output port of the FPGA. As input a start signal *write start* is initiated, to stream the *Comprressed Data* into the FPGA. At the output the corresponding *column* signals and *row* signals are generated. The main building blocks of the FPGA are the address controller, the ROM memories, one local video memory (RAM), and a multiplier-add engine.The address controller produces the addresses and the control signals to the dual port RAM memory and the two ROM memories. Additional control signals are generated for the multiplier add engine too. As the matrix $(F_n^T)^{-1}$ and the row matrix are composed of wavelet coefficients, they are independent of the incoming video data. Therefore they can be stored separately in the ROM memories. A dual port-RAM memory was used to minimize the size memory of the FPGA. This means that the write and read operations can be executed in the RAM once at the time if the write and read addresses are different.

The multiplier-add engine performs the matrix multiplication according to equation (1) to produce the column signals. The matrix multiplication is performed on a column sequential way as shown in Figure 3, which means that the column signals are computed in an order that allows them to be applied directly to the column drivers. This allows to minimize the size of the dual-port RAM memory to 220 pixels. During each line time, 110 pixels are written into the RAM memory, while in the same time110 pixels are read out of the RAM memory from the other 110 addresses. According to the way how the columns are computed as shown in Figure 3, it is required that the sample time of the read operations is 110 times faster than the write operations.

The calculated column signals and the row signals , corresponding to the outputs of the FPGA are then used to address the passive matrix display as shown in Figure 4.

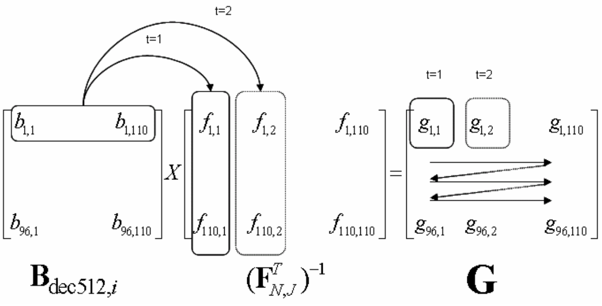

Figure 3. The column-sequential update of the column voltage matrix G.

To verify the visual quality between Figure 1 Left and Figure 4, it is interesting to make a measurement of the errors using equation (3)

$$error = \sum_{i=1}^{M}\sum_{j=1}^{N}\left|\tilde{x}_{ij} - x_{ij}\right|^{2} \qquad (3)$$

where x̃ij and xij represent the normalized reconstructed and the original pixel values respectively between one and zero. The dimension of the images is defined by $M \times N$ pixels, with i and j being used as parameters in the x and y direction respectively. The error values between Figure 1 and the original image is 5.5959 while the error between Figure 4 and the original image is 10.0998. Although the error metric is somewhat arbitrary it does show the effect of the quantization error in Figure 4. Those values show that the visual quality of the obtained display voltages using the hardware architecture is acceptable.

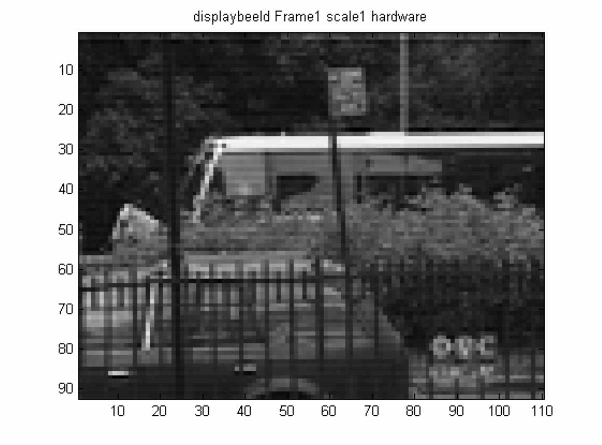

Figure 4. The obtained display voltages using the calculated column voltages and row voltages from the FPGA according to the architecture shown in Figure 2.

Afterwards the Xilinx Code Generator translates the Simulink model in vhdl code, from which the design in vhdl can be simulated in the behavioral simulator from Modelsim. The design flow is then followed by a synthesis compiler that supports the Xilinx device. After the synthesis step the configuration process of the FPGA generates the bitstream which is then loaded into the FPGA. The experiments were carried out using Spartan-3 FPGA Micromodule from Trenz Electronics[4]. To verify the correct operation of the design of the FPGA we used for simplicity a repeated test pattern instead of the video data as input to the FPGA. Based on the behavioral simulations with ModelSim, where the video stream input is replaced by a repeated testpattern in the Simulink model, we become the column signals and row signals, shown in Figure 5. These signals were then compared with the measured digital column and row signals at the output of the FPGA, shown in Figure 6 while at the input of the FPGA the same test pattern is applied using the Tektronix Function Generator, verifying the correct operation of the design of the FPGA.

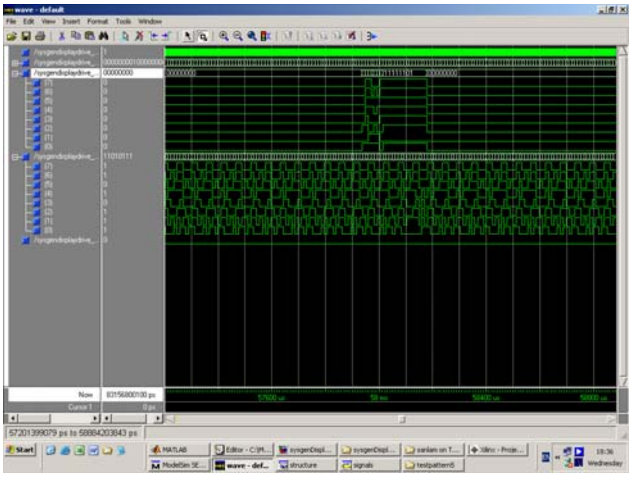

Figure 5. The 8 digital row signals on the upper half, and the 8 digital column signals on the bottom half, obtained with the behavioral simulation with Modelsim when a testpattern is applied to the FPGA in the Simulink model.

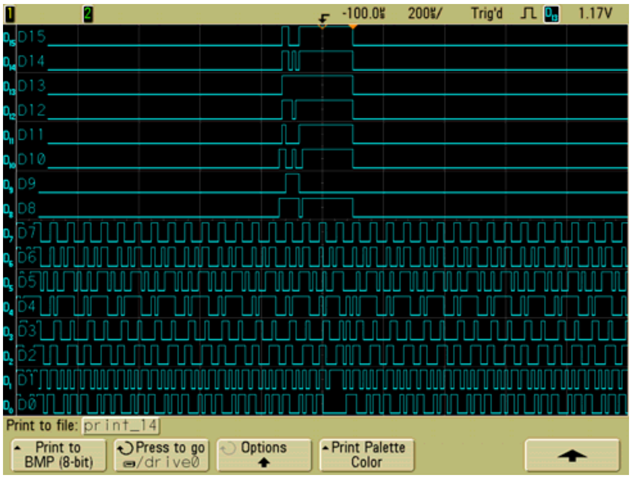

Figure 6. The 8 digital row signals on the upper half, and the 8 digital column signals on the bottom half, measured at the output of the FPGA when the same testpattern is applied to the input of the FPGA with the Tektronix function generator.

3. Conclusion

This paper describes the implementation of the proposed architecture presented in [1] using the FPGA of Xilinx. It is shown that the Simulink design flow for our FPGA application is a viable design path for our system. The design shows that our integrated architecture works well if the bit precision at the Gateway In and Gateway Out is high enough.

Another means to control the power consumption as mentioned in [5] is using the frame resolution scalable display addressing method. Dependent of the target resolution of displaying the media content on the passive matrix display, the hardware should be able to produce the column and row signals corresponding to the target resolution. An extra input bit to the FPGA defines the target resolution, in order to address the analysis matrices $(F_{n,J}^{T})^{-1}$ and row matrices of the right size in the ROM memories.This would enable the mobile terminal more flexibility in handling their power consumption.

4. Acknowledgements

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5. References

[1] S. Lam, H. De Smet, F. Verdicchio, A. Munteanu "Wavelet based moving picture coding multiple line addressing for passive matrix displays", *Proceedings 25th International Display Research Conference at Eurodisplay 2005, Edinburgh,* pp309-311(2004).

[2] Xilinx XBLOX and System Generator http://www.xilinx.com

[3] http://www.mathworks.com/applications/dsp_comm/xilinx_ref_guide.pdf

[4] http://www.trenz-electronic.de/prod/proden18.htm

[5] S. Lam, H. De Smet "Frame Resolution Scalability in Wavelet Based Multiple Line Addressing for Passive Matrix Displays"**.** *Society for Information Displays 2006 International Symposium Digest of Technical Papers.* Vol. 37. 2006. pp. 355-358