Design Considerations on Partition of SOP, CMOS and PCB technologies for Mobile Display System Implementation

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Abstract

For lower power and smaller size with higher image quality, it is desirable to have more units integrated on a display panel. It needs careful design considerations in selecting CMOS, SOP or PCB. An experimental display system is designed and power and delay considering chip area, data rates and bus width are analyzed for all technology combinations to obtain optimum design methodologies.

1. Introduction

Recently, multimedia mobile systems with display panels such as cellular phone, MP3, PDA and PMP become a general trend in consumer products. In the near future, more applications with a higher resolution and quality display panel will be desirable with low power, weight and size. To accomplish these, system on panel (SOP) with display systems integrated on a display panel is getting attentions as one of future display system technologies. In [1, 2], experimental display systems integrated on glass substrate have been reported. Furthermore, only main processor with multimedia extensions such as Bulverde or ARM is not enough to meet the requirements of various current application areas as well as image enhancements with varying standards. Also general purpose image processors require high hardware complexity with low efficiency not suitable for SOP. Therefore, a display image signal coprocessor is designed in this paper to be used in the SOP like wireless MMX [3]. Although the present status of SOP process yield is poor for commercial chip release, there have been improvements in minimum feature size and yield that can lead to SOP with image engines or processors integrated on a display panel in the future. Here, design considerations to decide the partition of SOP, CMOS and PCB implementation technologies for various units in a display system with expected performances is

essential. In this paper, multimedia mobile display system with ARM9 which is a typical main processor, display panel, peripheral circuits and an image coprocessor is designed to investigate optimum display system design methodologies and future SOP processing technology directions.

2. Test Bed Mobile Display System

Fig. 1 shows an overall architecture of the experimental SOP mobile display system.
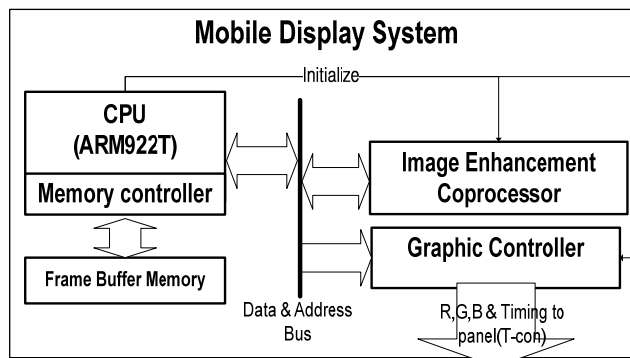

Fig. 1. Block diagram of mobile display system

ARM922T is used as a main processor for overall system controls and housekeeping tasks, the image coprocessor is dedicated to image processing computations, and the memory controller inside ARM controls the frame buffer memory. Graphic controller generates timing and RGB color signals.

3. Analyses on Image Data Transfer Behaviors

Interface bus widths and operating clock frequencies of each module in test bed mobile display system are summarized and data transfer activities on the interfaces are investigated as shown in Table 1.

TABLE 1. Interface clock frequencies, bus width and activity rate

Interconnection	Operating clock	Bus width	Activity rate
Coprocessor → Memory controller	25MHz 125MHz	64	0.00135
Memory controller → Coprocessor	125MHz 25MHz	64	0.00300
Frame buffer → Memory controller	83.33MHz 125MHz	47	0.00492
Memory controller → Frame buffer	125MHz 83.33MHz	47	0.00128
Memory controller → Graphic Controller	125MHz 25MHz	64	0.00122
Graphic Controller → Panel	25MHz 4.16MHz	24	0.01167

In analyzing frame buffer interface bus width, the 15 bit addresses and 32 bit data are estimated and relatively fewer control signals are excluded. Activity rate estimating average interface data usage for data transfer is defined as below.

Activity rate = # of active clock cycles / # of total clock cycles

To maximize switching of experimental data, repetitive pattern of 0 and 1 data are generated by using 0xAAAAAAAA and 0x55555555 as memory input. Test bed mobile display system is simulated with 32 pixels by 16 lines as a frame. When the system displays 1 frame data, first, the image coprocessor executes pack operation [4] and the data is stored in the frame buffer, then graphic controller displays the resulting data. The delay of 9ms is inserted between the operation of the coprocessor and the graphic controller to separate the influence of each of them clearly.

Also, the patterns of average data rate for each interface in every 1 us are investigated as shown in Figure 2. The behavior of data rate shows pattern A generated due to the burst data transfer to receive the image data to execute pack command in the coprocessor, then store back to the frame buffer (coprocessor – memory controller, memory controller – frame buffer). The data rate pattern B, sudden increase of data rate, is generated by burst transfer from the frame buffer (frame buffer – memory controller, graphic controller – memory controller, graphic controller – panel interface) to display image data after the pack execution.
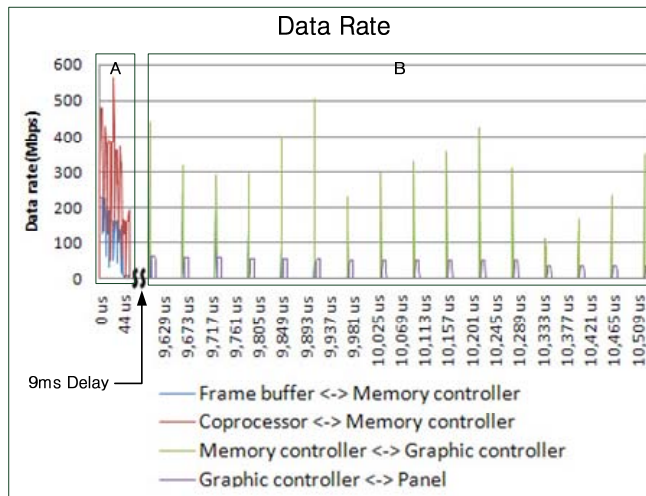

Fig. 2. Data rate patterns

To investigate the data transfer behaviors based on each processing technology, the performance analyses of power and delay are estimated based on 1 bit interconnection using the parameters of [5-7] for CMOS, LTPS SOP and off chip interfaces as shown in Figure 3.
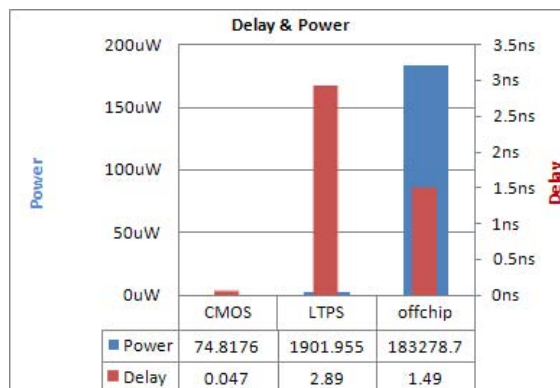

	CMOS	LTPS	offchip
Power	74.8176	1901.955	183278.7
Delay	0.047	2.89	1.49

Fig. 3. Delay and power comparisons of CMOS, LTPS and off chip interconnections.

CMOS interconnection shows the superior performance. LTPS is good in power consumption, but the delay is very high, demerits on interfaces with high activity rate and data rate with instantaneous peaks.

Table 1 shows high activity rate at interfaces of frame buffer – memory controller, memory controller - coprocessor and graphic controller – panel. From instantaneous date rate point of views, all of the interface interconnections connected to the memory controller always show sharp instantaneous peak as shown in Figure 2. To implement such interconnections with LTPS, the delay of the interconnection should be improved.

4. PERFORMANCE EVALUATIONS ACCORDING TO PARTITIONS OF SOP, CMOS AND PCB

To compare performances, all possible 6 partition cases are listed in Table 2.

TABLE 2. 6 Partition plans

Partitions	CMOS	LTPS
Partition Ⅰ (Conventional system)	Frame Buffer ARM core (Memory controller) Graphic controller Coprocessor	Display Panel
Partition Ⅱ	Frame Buffer ARM core (Memory controller) Graphic controller Coprocessor	Display Panel
Partition Ⅲ	Frame Buffer ARM core (Memory controller) Coprocessor	Display Panel Graphic controller
Partition Ⅳ	Frame Buffer ARM core (Memory controller)	Display Panel Graphic controller Coprocessor
Partition Ⅴ	Frame Buffer	Display Panel Graphic controller Coprocessor ARM core (Memory controller)
Partition Ⅵ	None	Display Panel Graphic controller Coprocessor ARM core (Memory controller) Frame Buffer

Since the SOP process is inferior to CMOS requiring much chip area, Table 2 shows partition plans in accordance with total chip area. In Table 2, if the system is implemented with the same technology with separate chips, separate chip is shown with shaded area requiring off chip interconnections. As discussed before, careful consideration about delay is necessary for frame buffer – memory controller interface and coprocessor – memory controller interface due to high data rate.

Considering data rate, interface delay and power of each partition scheme, instantaneous powers are illustrated as shown in Figure 4.
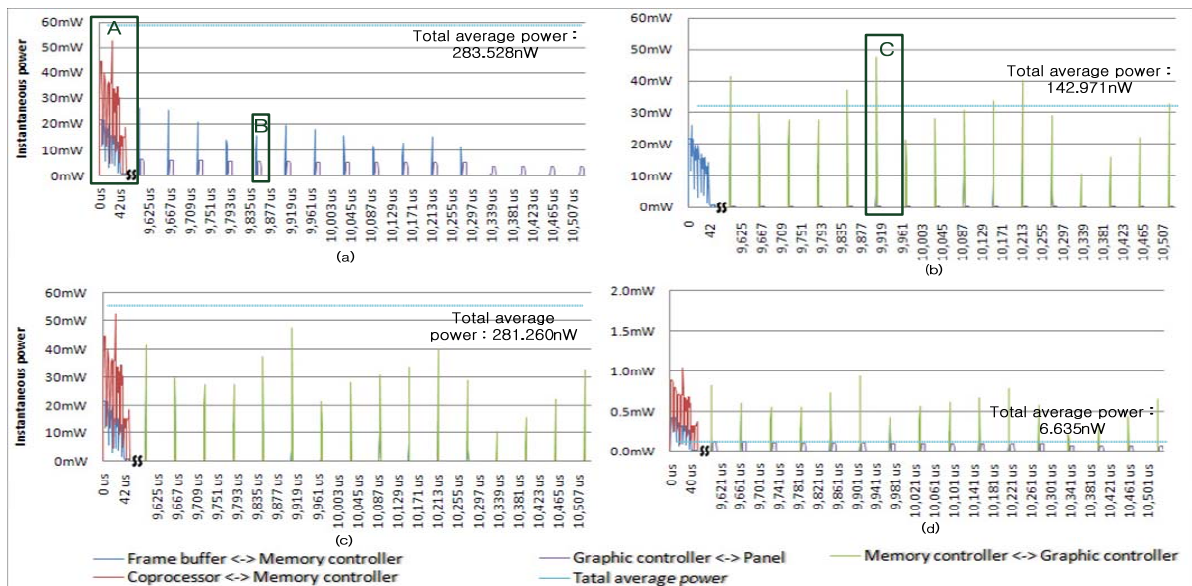

Fig. 4. Comparisons of Instantaneous and average powers.
a) Partition Ⅰ b) Partition Ⅲ c) Partition Ⅳ d) Partition Ⅵ

A, B in Figure 4 (a), and C in Figure 4 (b) show burst data pattern of coprocessor – memory controller interface, graphic controller – panel interface, memory controller – graphic controller interface, respectively, similar to the data rate patterns shown in Figure 2. If these interfaces are implemented with off chip, high power consumption with sharp peak instantaneous power pattern appears and it can be reduced greatly

with on chip implementation or interconnections.

The comparisons of total power consumptions and relative power saving for each partition case compared to partition Ⅰ are shown in Figure 5.
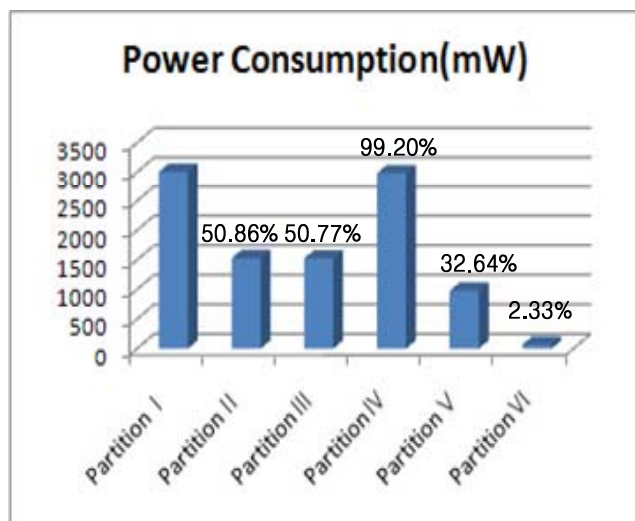

Fig. 5. Total power consumption

Total power consumption can be categorized as partition Ⅱ, Ⅲ, Ⅴ group, partition Ⅰ, Ⅳ group and partition Ⅵ according to how much interfaces from memory controller to adjacent modules except display panel are interconnected with off chip interconnections. The power savings, the advantage of SOP cannot be achieved even if system modules are implemented with SOP as long as the memory controller with high data rate is implemented with off chip interconnections as shown in partition Ⅰ and Ⅳ in Figure 5. This needs to be carefully considered in the early design phase. As long as interfaces connected to memory controller are implemented with on chip SOP or CMOS, power is reduced as shown in partition Ⅱ, Ⅲ, Ⅴ group, but the power is not reduced below a certain level because frame buffer – memory controller interface is still implemented with off chip interconnections. As frame buffer – memory controller interface is implemented with on chip or SOP, the power consumption is dropped rapidly down to 2.33% compared to partition I. Therefore, if the image memory is implemented with on chip SOP, it can improve system performance greatly. Based on the analysis results above, the critical module such as memory controller with high connectivity of interfaces, data rate and activity rate should be implemented with the same technology as well as on chip interconnections.

5. Conclusion

An experimental mobile display system is designed to develop optimal display system implementation methodologies with CMOS, off the shelf and costly SOP processes. Considering data transfer patterns and activities as well as the delay and power consumption of CMOS, SOP, off chip PCB interconnections, six partition cases are investigated. Large delay of SOP on chip interconnections need to be improved for high data rate interfaces. Memory controller with higher connectivity and data transfer activities has the most impact on power consumption, which requires on chip interconnection regardless of CMOS or SOP. In addition, modules such as frame buffers need to be implemented with SOP. As a result, SOP integration needs to be carefully planned in the early design phase considering all the interfaces minimizing cost and power and maximizing system performances.

6. References

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