Formation of Buffer Layer on Mica for Application to Flexible Thin Film Transistors

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Abstract

A buffer layer consisting of SiO_x/Ta/Ti has been developed in order to overcome the adhesion and stress problems between poly-Si film and mica. Polycrystalline silicon thin film transistor was successfully fabricated on the mica and transferred to a flexible plastic substrate.

1. Introduction

To fabricate poly-Si TFTs on plastic substrates, direct low temperature poly-Si (LTPS) technology and layer transfer technology have been utilized. The maximum temperature in the direct LTPS process on plastic substrates must be lowered below plastic glass transition temperature at 150~250℃, the point at which the substrate loses its thermal and mechanical integrity. Therefore, it is too difficult to apply conventional process for fabricating poly-Si TFTs on plastic substrates[1]. On the other hand, the layer transfer technology has been developed in order to obtain the poly-Si TFTs on plastic substrates by the conventional process. There are no limitations of the process temperature because chemically and thermally durable mother substrate is used. However, techniques for the separation of the poly-Si TFTs from the mother substrate are necessarily required[2-4].

In this work, the muscovite mica was chosen as the mother-substrates for layer transfer technology of poly-Si TFTs. The mica is not only replaceable to the plastic substrate due to its flexibility, transparency, chemical stability and relatively high temperature resistance (below 600℃), but also easily cleaved into thin plates. However, there were several problems such as delamination and cracking of the deposited films on the mica during the fabrication of poly-Si TFTs. Therefore, the novel buffer layer composed of SiO_x/Ta/Ti thin film was induced between the mica substrate and poly-Si TFTs. The SiO_x layer is for electrical isolation, the Ti layer is for adhesion of SiO_x and mica, and Ta is for the protection of Ti. Using this buffer layer, poly-Si TFTs were successfully fabricated on the mica substrate and transferred on plastic substrate.

2. Experimental

(1) Material selection for buffer layer

The films deposited on the mica substrate are likely to be delaminated and exfoliated due to the poor surface adhesion of the mica, leading to deteriorate the manufacturing stability of devices. Therefore, the buffer layer composed of SiO_x/Ta/Ti thin film was induced between the mica substrate and poly-Si TFTs. The SiO_x layer is for electrical isolation, the Ti layer is for adhesion of SiO_x and mica, and Ta is for the protection of Ti. Moreover, thermal expansion coefficient (TCE) of these materials was also considered for the selection of the buffer layer on the mica substrate. From the measurement of TCE using thermal-mechnical analyzer (TMA) at a temperature range of 40~200℃, TCE of the mica was obtained at 10 ppm/℃, which is 1/7~1/5 lower than the conventional plastic substrates such as PET and PES. TCE values of Ti, Ta, SiO_x are 8.6, 6.3, 3.5~4.1 ppm/℃, respectively. Therefore, the structure of the buffer layer consisting of SiO_x/Ta/Ti thin film was designed for the difference of TCE between the thin films and mica to decrease by 2 ppm/℃.

(2) Formation and characterization of the buffer layer

A Ti adhesion layer was deposited on the mica substrate at a room temperature by DC magnetron sputtering, varying the working pressure in the range of 2~20 mtorr. After the deposition of Ti, the Ta protective layer with the thickness of 50 nm was *in-situ* deposited on the Ti adhesion layer at 4 mtorr. Finally, the SiO_x isolation layer with the thickness of

300 nm was formed on the Ta protective layer at 200℃ by PECVD.

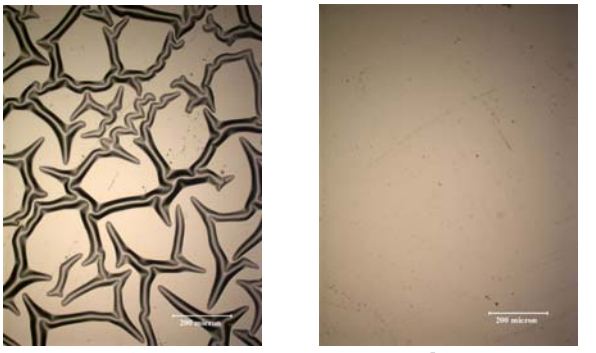
The surface morphology of the buffer layer was observed by the optical microscopy (OM), and its cross-sectional structure was confirmed by scanning electron microscopy (SEM). The crystal structure of the buffer layer was determined by x-ray diffraction (XRD) and the film stress was analyzed using the high-resolution XRD (HRXRD).

3. Results and discussion

Ti layer (adhesion layer) was deposited on the mica substrate by DC magnetron sputtering in various working pressure conditions from 2 to 20 mtorr and its thickness was fixed at 3000 Å. Figure 1 shows optical micrographs of as-deposited Ti layer at (a) 2 mtorr and (b) 5 mtorr. It is seen that the Ti layer deposited at 2 mtorr is very unstable on the mica and thin film failure such as delamination and peeling-off occurs. But, the Ti layer deposited at above 5 mtorr is stable on the mica substrate. This seems to be related to residual stress of the Ti layer. The residual stress in the Ti layers was analyzed using a Psi-tilting method by high-resolution XRD. Figure 2 shows the residual stresses of the Ti layers as a function of working pressure. The residual stress in the Ti layer between 2 mtorr and 5 mtorr is dramatically changing from -800 MPa (compressive stress) to +800 MPa (tensile stress). This indicates that the adhesion of the Ti layer on the mica is dependent on its residual stress. Therefore, it is confirmed that the tensile stressed Ti layer (deposited at above 5mtorr) is suitable to enhance the adhesion on the mica.

Figure 3 shows the optical micrographs of samples with (a) SiO_x/Ti buffer layer and (b) SiO_x/Ta/Ti buffer layer on the mica substrate after dipping Si etchant. It is clearly seen that sample without the Ta layer between Ti adhesion layer and SiO_x isolation layer is very unstable, and the cracking and peeling-off of the buffer layer are observed. It seems that the surface damages in Fig. 3(a) are due to the etching of Ti layer by Si etchant, which can penetrate through lots of pin-holes within the SiO_x isolation layer and react intensely with the Ti adhesion layer. However, from Fig. 3(b), there were no surface damages in the sample with the Ta layer between Ti adhesion layer and SiO_x isolation layer. Its surface was very clean. Therefore, it is confirmed that the Ta layer is able to protect the Ti adhesion layer from many kinds of chemicals.

Figure 4 shows the XRD patterns of the SiO_x/Ta/Ti buffer layer on the mica substrate as a function of the annealing time for metal-induced crystallization of a-Si. It was seen that there was no reaction between Ti layer and Ta layer although the sample was annealed at 550℃ for 25h (Fig 5). And, as not shown in this paper, no thin film failure such as delamination, peeling-off, and cracking was observed. This implies that the buffer layer is very stable and offers wide process range for the fabrication of poly-Si TFTs on the mica. Finally, poly-Si TFTs fabricated on the mica were successfully transferred to PES substrate, as shown in Figure 6.



(a) (b)

Fig. 1. Optical micrographs of as-deposited Ti layer at (a) 2 mtorr and (b) 5 mtorr.

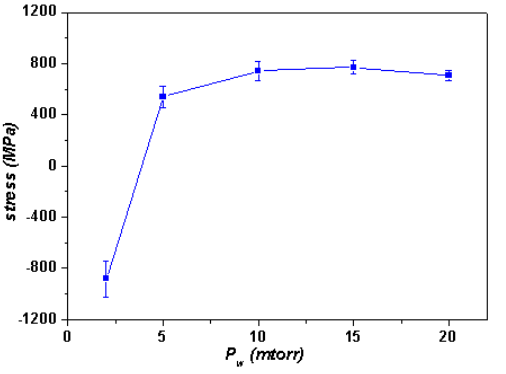
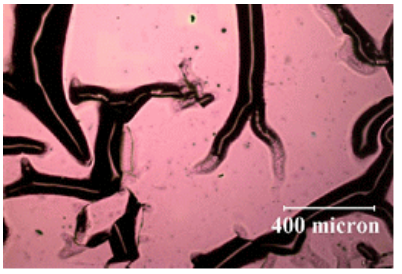
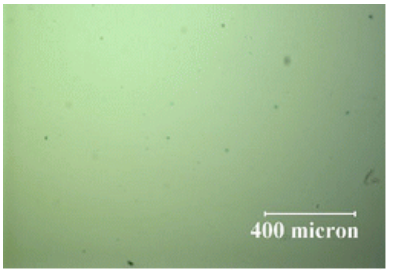


Fig. 2. Residual stress of as-deposited Ti layers as a function of working pressure.



(a)



(b)

Fig. 3. Optical micrographs of samples with (a) SiO_x/Ti buffer layer and (b) SiO_x/Ta/Ti buffer layer after dipping in Si etchant.

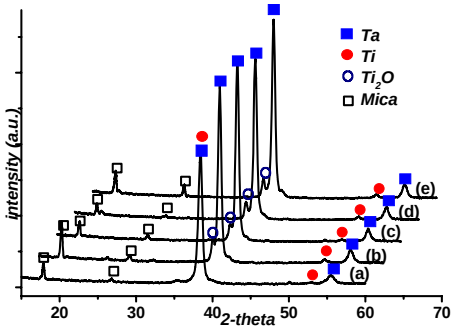


Fig. 4. XRD patterns of (a) the as-deposited buffer layer and the buffer layer annealed at 550℃ for (b) 1h, (c) 5h, (d) 15h, and (e) 25h.

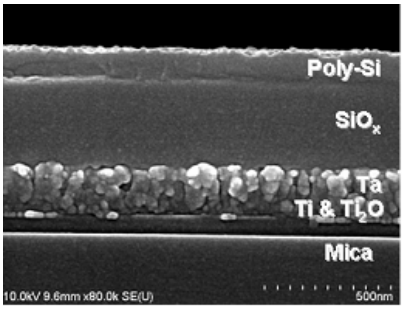


Fig. 5. Cross-sectional SEM image of crystallized Si on the SiO_x/Ta/Ti buffer layer/mica substrate.

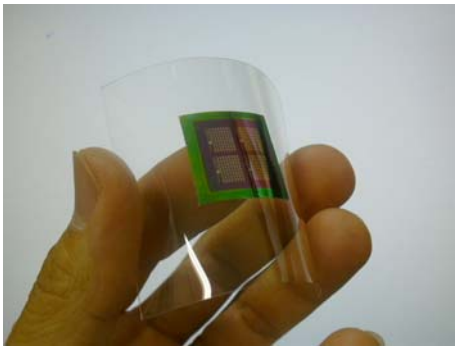


Fig. 6. Transferred poly-Si TFTs on PES substrate.

4. Summary

This study is a new attempt for poly-Si TFTs on a mica to apply the flexible display. The mica has never been used as the substrate material for the fabrication of the poly-Si TFTs. However, there are several problems such as delamination and cracking of the deposited films on the mica during the fabrication of poly-Si TFTs. Therefore, the novel buffer layer consisting of SiO_x/Ta/Ti thin film is induced between the mica and poly-Si TFTs for the first time. Using this buffer layer, we can fabricate the poly-Si TFTs on the mica and easily transfer on the plastic substrate.

5. References

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