3.5 inch QCIF AMOLED Panel with Ultra Low Temperature Polycrystalline Silicon Thin Film Transistor on Plastic Substrate

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Abstract

We fabricated the 3.5 inch QCIF AMOLED panel with ultra low temperature polycrystalline silicon TFT on the plastic substrate. To reduce the leakage current, we used the triple layered gate metal structure. To reduce the stress from inorganic dielectric layer, we applied the organic interlayer dielectric and the photoactive insulating layer. By using the interlayer dielectric as a capacitor, the mask steps are reduced up to five.

1. Introduction

Flexible displays are currently the subject of a great deal of interest due to their low weight, superior compactness, robustness and design flexibility compared with conventional glass-based displays. In order to realize a mechanically stable display, however, several issues must be resolved [1].

Inorganic materials have very different mechanical properties compared with plastic substrates; therefore, cracking and delamination may occur during the fabrication process and in operation. Furthermore, the thermal expansion coefficients of plastic substrates are much larger than those of inorganic materials and consequently, stresses during the deposition process are introduced. If a freestanding substrate is employed, the curvature of the inorganic film structures on plastic substrates changes during circuit fabrication, causing misalignment between the layers. In order to prevent this misalignment, the plastic substrate is typically bonded to a rigid carrier.

The adhesive used for bonding the plastic substrate must withstand the TFT process temperatures and chemicals; therefore, the use of an adhesive necessitates a reduction of the maximum process temperature from the value that the substrate itself would normally withstand. The aforementioned issues as well as the low thermal resistance of most plastic substrates necessitate an ultra low temperature poly-Si (ULTPS) TFT process [2,3,4].

In this work, we present the key process for integrating the 3.5 inch QCIF active matrix organic light emitting diode (AMOLED) panel with ULTPS TFT on the plastic substrate.

2. Experimental

Fig. 1 shows the optical microscopy image of unit cell. The unit cell is designed with 10 ㎛ design rule and five mask processes are achieved by using interlayer dielectric layer as capacitor. The unit cell size is 390 ㎛ x 390 ㎛.

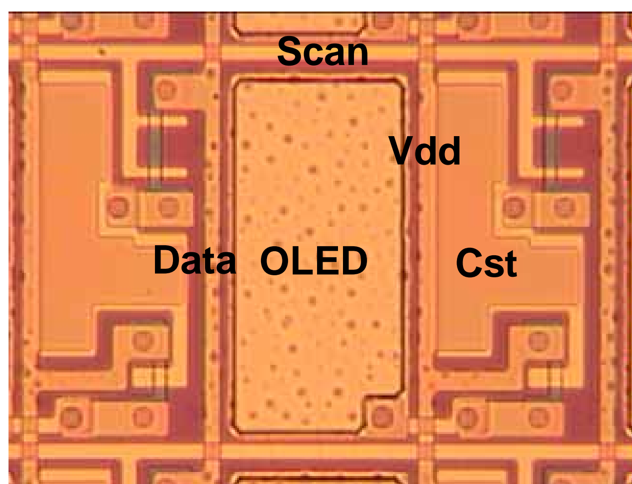

Fig. 1. Optical microscopy Image of Unit Cell.

The process steps are as follows: The plastic substrate. polyarylites (PAR), is attached to the glass carrier wafer with an adhesive of 600 gf/inch peel strength. If the adhesive strength is weak, the plastic substrate is delaminated due to the thermal and mechanical stress. To prevent damage on the plastic substrates during the laser dopant activation, the oxide-silicon-oxide (SiO_2-Si-SiO_2) buffer structure was used [5]. We deposited an 80 nm thick a-Si film on the buffer layer as an active layer which is crystallized by sequential lateral solidification (SLS).

Prior to the oxidation, the surface of the Si substrate was cleaned with a 100:1 hydrofluoric acid solution to remove the native oxide layer. We attempted to oxidize the Si surface with a pulsed O_2 plasma at a RF frequency 13.56 MHz and a power of 0.41 W/cm^2 for 30 min in the PEALD chamber. A gate dielectric Al_2O_3 film containing nitrogen (< 1 %) was deposited *in situ* with the O_2 gas mixed with N_2 gas as the oxidants and trimethylaluminum as the source of Al [6].

To reduce the leakage current of TFT, we adopted the triple layered gate metal structure as shown in fig. 2 which is effective in reducing the electric field at the gate edge.

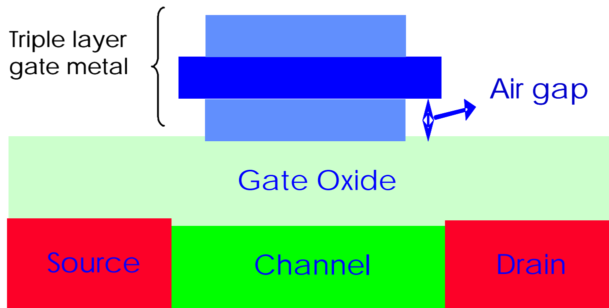

Fig. 2. Schemetic TFT structure of triple layer metal gate with 20nm Al/20nm Cr/150 nm Al.

The triple layered metal is consisted of 20 nm Al/20 nm Cr/150 nm Al and the air gap is made with overetching of the Al metals. Top Aluminum layer is require to protect the damage during the laser activation. After the patterning of the gate electrode, the p+ source and drain (S/D) regions were formed and activated.

We used the organic interlayer dielectric of low dielectric constant. Because the low thermal budget is necessary, we developed the new material of low temperature below 120 °C. It is used as the interdielectric material to prevent the shortage of the data line and the scan line as well as the capacitor between the S/D metal and the gate metal to reduce the mask step as well as the process stress.

The S/D metal is formed with 10 nm Cr/200nm Al/10nm Cr by DC sputtering. It acts as the S/D metal as well as the anode metal. The bottom Cr metal is used for the adhesion promotion layer and the top Cr metal is used for the work function matching layer to the hole injection layer of OLED film.

The bank layer is made of the photoactive insulating layer (PIL) as shown in fig. 3. By using the thick PIL layer, we can protect the shortage between the anode metal and the cathode metal. The Slope of the bank is lower enough to confirm the uniform OLED evaporation at the bank edge which is necessary to reduce the OLED leakage current.

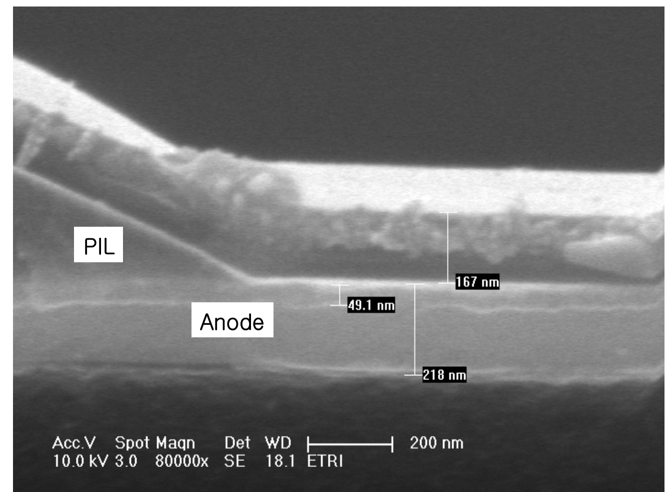

Fig. 3. The SEM image of the Bank layer which is made of photoactive insulating layer.

The device structure of an OLED was grown by vacuum thermal deposition is 10 nm 2-TNATA/30 nm a-NPB/30 nm Alq:C545T/30 nm Alq. The transparent cathode metal is composed of 1 nm LiF/1 nm Al/15 nm Ag. The bi-layer of a-NPB and LiF deposited by thermal evaporation and some inorganic layers including AlOx grown by ALD were used for thin film encapsulation [7].

3. Results and discussion

Fig. 4 shows the leakage current characteristics of TFT between of the single layered metal and of the triple layered metal. Although the threshold voltage of triple layer metal structure is increased by 2V, the leakage current is reduced by 1 order at V_G=5V.

Furthermore the rate of leakage current increase as a function of gate voltage is drastically reduced. The leakage current of the poly-Si TFT is mainly explained by the electric field induced leakage current. The lower slope means the lower electric field at the gate edge.

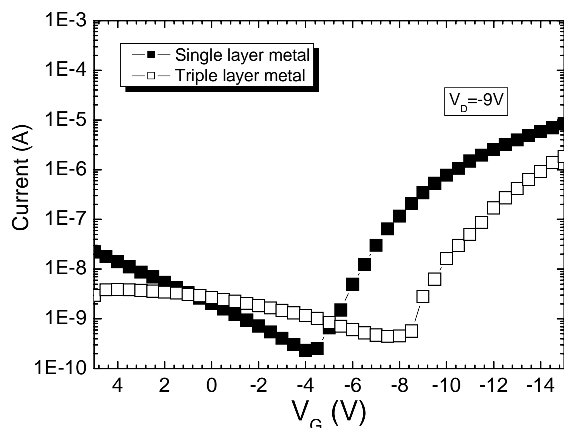

Fig. 4. Leakage current characteristics between of the single layer metal and of the triple layer metal..

Fig. 5 shows the capacitance characteristics of the organic interlayer dielectric as a function of frequency with the dielectric constant of 3.16. Although the baking temperature of the organic interlayer dielectric is below 120 ^{o}C, the leakage current is below 1E-8 A/cm^2 at 1MV/cm.

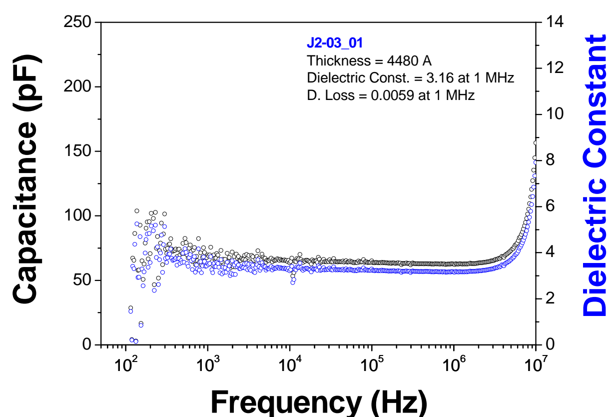

Fig. 5. Capacitance characteristics of Organic interlayer dielectric.

The 3.5 inch QCIF AMOLED panel is shown in fig. 6. Although the improvement of the panel uniformity and the defect control is more required, the panel shows the flexibility of the substrate.

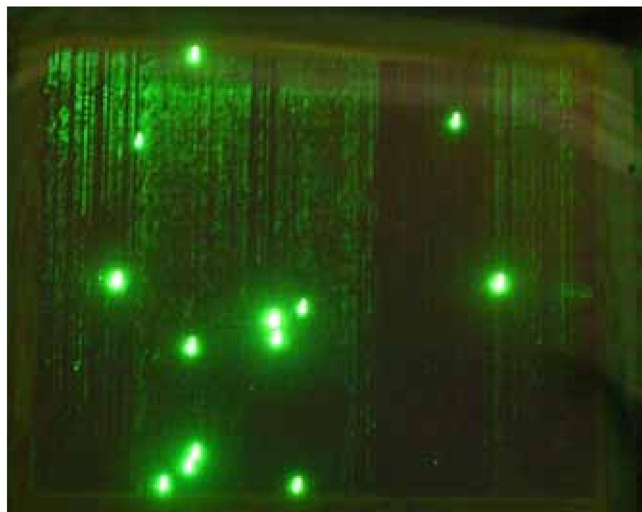

Fig. 6. 3.5 inch QCIF AMOLED panel characteristics.

4. Summary

We fabricated the 3.5 inch QCIF AMOLED panel with ultra low temperature polycrystalline silicon TFT on the plastic substrate. By using the triple layered gate metal structure, we can reduce the leakage current. The newly developed organic interlayer dielectric layer shows the low leakage current in spite of the low thermal budget. By using the interlayer dielectric as a capacitor, the mask steps can be reduced up to five step.

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