Load Current Prediction Method for a DC-DC Converter in Plasma Display Panel

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Abstract

This paper describes a new method to predict the load current of a dc-dc converter. The load current is calculated using the video information of the PDP. The output capacitance of the dc-dc converter can be reduced by utilizing the predicted load current, which results in a cost reduction of the power system in the PDP.

1. Introduction

The Plasma Display Panel (PDP) requires a large amount of discharge current during the sustain period for displaying the image data. The peak value of the discharge current is in the range of 0A to 100A and the frequency is the same as that of the sustain pulse. To supply the pulsating discharge current immediately, input filters are normally inserted between the dc-dc converter and the driving circuit of the PDP.

The main role of the dc-dc converter is to supply the load current with the tightly regulated dc output voltage. The load current is the filtered discharge current of the PDP. As the periodic type driving scheme as ADS [1] is widely used in the PDP, the load current of the dc-dc converter continuously changes from no load to full load within 1 TV field.

The common method to meet the tight voltage regulation specification at this varying load condition is to increase the output capacitance of the dc-dc converter. But if we can use the predicted load current information as a feed-forward function in addition to the feed-back controller, the output capacitance can be reduced while maintaining the output voltage variation at the lower level.

This paper introduces the load current prediction method of the PDP without a separate sensing network. The load current is predicted based on the internal video information and gate signals of the full bridge panel driving circuit. The load current prediction method and control algorithm of the dc-dc converter are implemented digitally using an FPGA.

A 400W dc-dc converter with a 42inch HD PDP is used for the experimental verification.

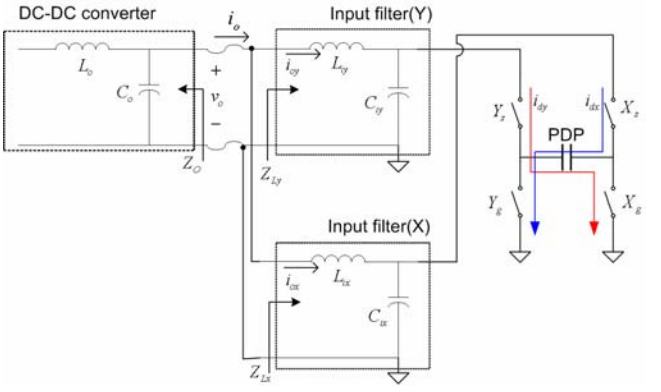

Fig. 1. Circuit structure

2. Prediction Method

A. Discharge current and input filters

Figure 1 shows the basic circuit structure, which includes the dc-dc converter and the full bridge panel driving circuit with input filters. The current transfer function between the discharge current and the filtered current shows the low pass filter characteristics. The transfer function of the X driving circuit is represented as

$$i_{odx}(s) = \frac{i_{ox}}{i_{dx}} \simeq \frac{1}{1 + s^2 C_{ix} L_{ix}} \qquad (1)$$

where L_{ix} is the inductance and C_{ix} is the capacitance of the input filter. It is assumed in Eq.(1) that the input

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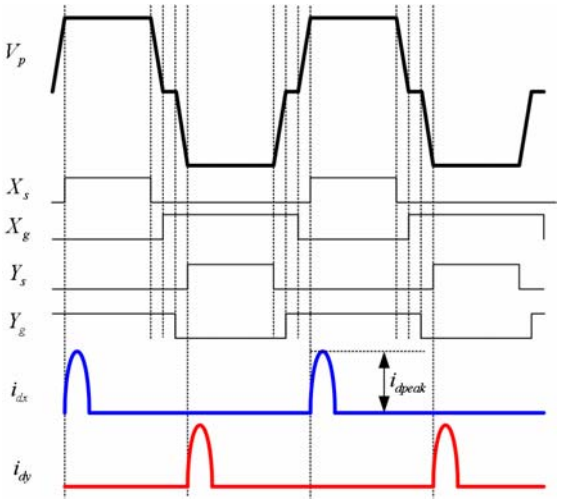


Fig. 2. Sustain pulse and discharge current

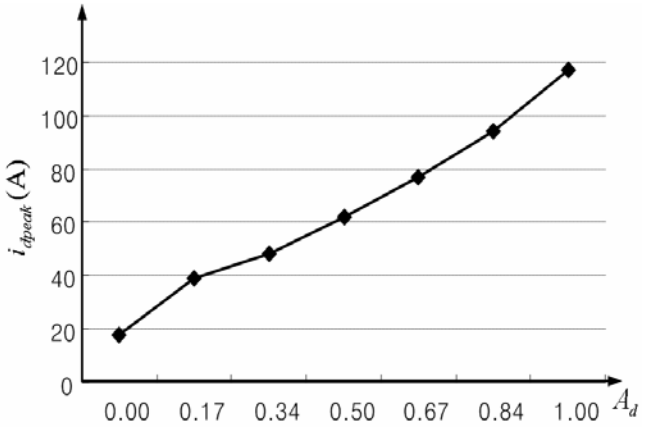


Fig. 3. Discharge current and area

impedance of the input filter, Z_{Lx}, is designed to be larger than the output impedance of the dc-dc converter, Z_o, to avoid interaction. Similarly, the transfer function of the Y driving circuit is

$$i_{ody}(s) = \frac{i_{oy}}{i_{dy}} \simeq \frac{1}{1 + s^2 C_{iy} L_{iy}} \tag{2}$$

It is observed in Eq.(1) and Eq.(2) that the high frequency pulsating discharge current is converted to a low frequency current by the input filter. Then the load current of the dc-dc converter, i_o, is given by

$$i_o = i_{ox} + i_{oy} \tag{3}$$

where i_{ox} and i_{oy} are the low pass filtered discharge current of the X and Y driving circuits.

In the case of the ADS driving scheme, 1 TV filed is

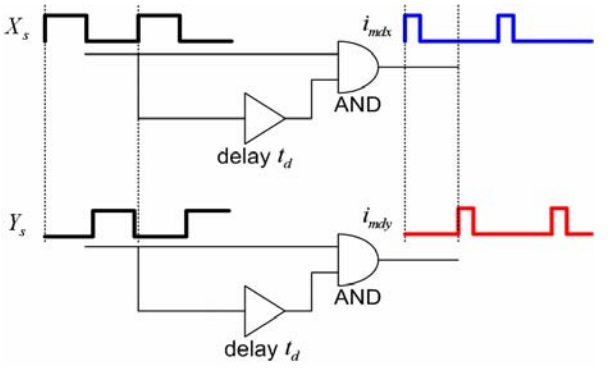


Fig. 4. Modeling of the discharge current

normally composed of 8 to 12 subfields. The discharge area of each subfield is determined by the input video information. The amplitude of the discharge current is proportional to the discharge area of each sub-field, and the frequency of the current coincides with the frequency of the sustain pulse. The sustain pulse, V_p, is generated by the full bridge circuit controlled by the gate signals as shown in Fig.2.

During each sub-field, the amplitude of the discharge current, i_{dpeak}, is almost constant and the number of i_{dpeak} is the same as that of the sustain pulse. The ratio of the discharge area, A_d, in each subfield is represented by

$$A_d = \frac{S_a}{3 \bullet R} \tag{4}$$

where R is the resolution of the PDP and S_a is the selected cells for the address discharge.

Figure 3 shows the measured amplitude of the discharge current, i_{dpeak}, in a 42 inch HD PDP as a function of the discharge area, A_d. It can be observed that the amplitude is proportional to the ratio of the discharge area. The measured i_{dpeak} is saved as a lookup table and indexed by A_d during operation for the digital modeling of the discharge current.

B. Digital modeling and load current prediction

The position information of the discharge current is obtained by a simple logical combination of gate signals as shown in Fig.4.

The position of the discharge current in the Y driving circuit, i_{mdy}, is the result of a logical AND operation of the high side gate signal, Y_s, and delayed Y_s. The delay time, t_d, is fixed to the value of 700ns by

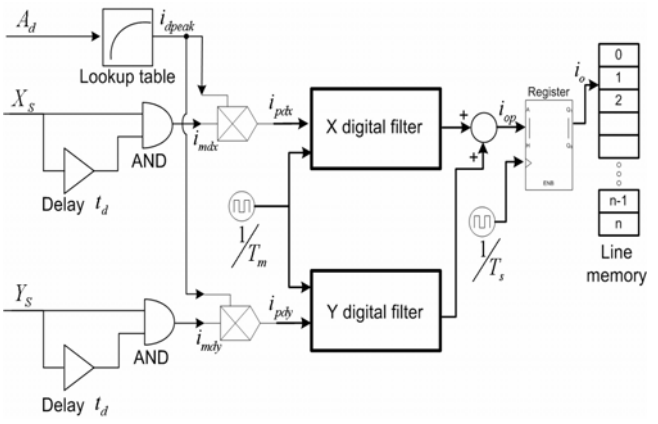


Fig. 5. Block diagram of the prediction method

considering the width of the maximum discharge current. The same method is applied to model the position of the discharge current in the X driving circuit, i_{mdx}.

Figure 5 shows the overall structure of the digital load current prediction method. The digitally modeled discharge currents, i_{pdx} and i_{pdy}, are calculated by multiplying the amplitude i_{dpeak} and the position of the discharge currents, i_{mdx} and i_{mdy}. Then i_{pdx} and i_{pdy} are used as inputs to the X and Y digital filters.

By applying the z-transform to Eq.(1), the transfer function of the X digital filter is

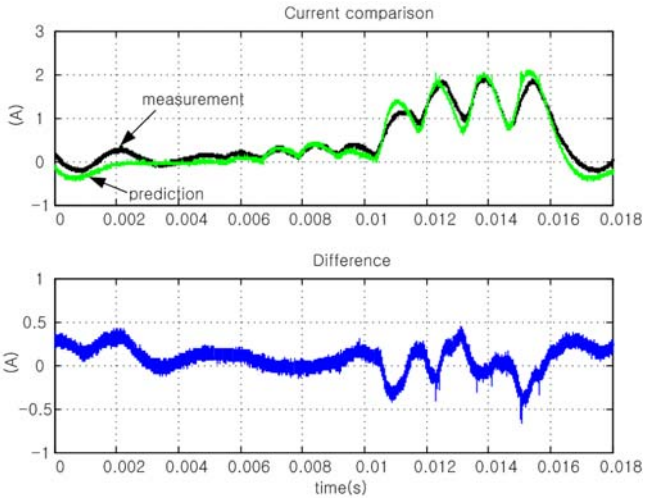
$$i_{odx}(z) = \frac{\left(1-\cos\left(w_{fx}T_m\right)\right)(z+1)}{z^2 - 2z\cos(w_{fx}T_m)+1} \text{ where } w_{fx} = \frac{1}{\sqrt{L_{ix}C_{ix}}} \quad (5)$$

From Eq.(2), the transfer function for the Y digital filter is

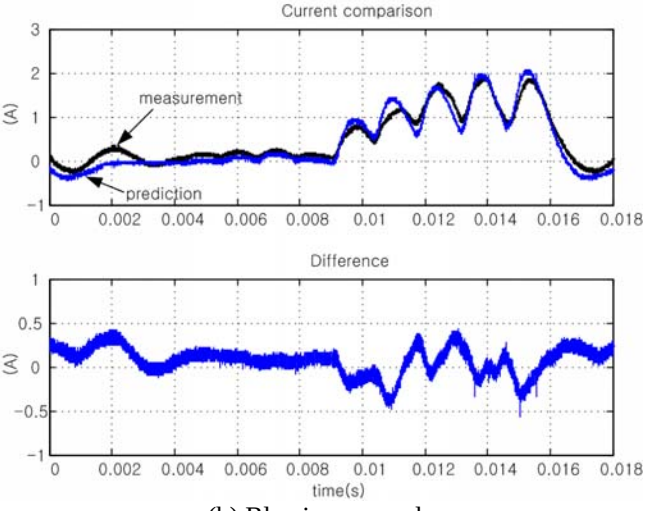
$$i_{odx}(z) = \frac{\left(1-\cos\left(w_{fy}T_m\right)\right)(z+1)}{z^2 - 2z\cos(w_{fy}T_m)+1} \text{ where } w_{fy} = \frac{1}{\sqrt{L_{iy}C_{iy}}} \quad (6)$$

The sampling period, T_m ,of Eq.(5) and Eq.(6) is designed to be shorter than the delay, t_d, in order to detect the digitally modeled discharge current at least once per period.

By summing the filtered result of Eq.(5) and Eq.(6), we can predict the load current. The predicted load current, i_{op}, is re-sampled by the switching period, T_s, of the dc-dc converter and saved in the line memory. The saved data is utilized in the next TV field to enhance the regulation performance of the dc-dc converter.



(a) Green image mode



(b) Blue image mode

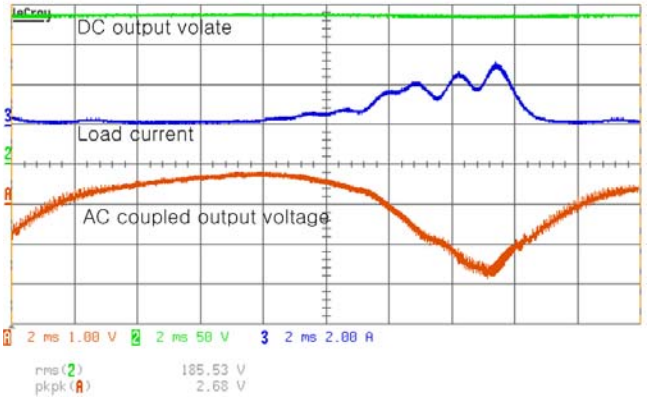
Fig. 6. Current prediction and measurement

3. Experimental results

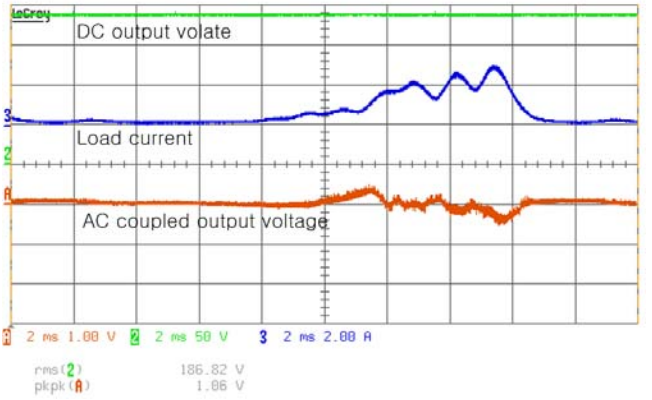
The proposed digital load current prediction method is implemented using a Xilinx Spartan-III FPGA. The digital control algorithm of the dc-dc converter is also implemented on the same FPGA.

Figure 6 compares the predicted and measured load currents. The experiments are executed with a 42 inch HD PDP displaying the green and blue image on the screen. In both image modes, the predicted load current tracks the real load current to within 20% error.

The control of the dc-dc converter is based on the digital feed-forward controller [2] using the predicted load current. The predicted load current is used to calculate the required duty ratio of the dc-dc converter.



(a) C_o=2mF with conventional feedback control



(b) C_o=440uF with load current feed-forward control

Fig. 7. Output voltage variation

The regulation performance of the dc-dc converter is compared in Fig. 7. It is observed that the load current feed-forward control method with a small output capacitor reduces the output voltage variation by 60% compared to the conventional feedback [3] control method with a large output capacitor.

4. Summary

This paper introduces the load current prediction method without a separate sensing network in the PDP. The load current is predicted using the digital filter, the discharge area of each subfield and the gate signals of the full bridge panel driving circuit. It is shown through the experiments that the error between the predicted and measured load current is maintained in the range of 20%. The predicted load current is used to minimize the output voltage variation of the dc-dc converter which supplies power during the sustain period. A low cost and high quality PDP power system can be realized by using the proposed load current prediction concept.

5. References

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3. A. Prodic, D. Maksimovic, R.W. Erickson, “Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter”, in Proc. IEEE IECON., 2001, pp.893-898.