Investigation on the Flicker for the Optimal Design of LCD Panel

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Abstract

In this paper, we present a novel method to minimize flicker and gray scale errors automatically across the entire panel by using a compensation of the gray levels of image. It was realized by image simulation with feedback structure. As a result of simulation, we observed flickers from the simulated image. And we compensated the gray scale levels for original image. The compensated gray scale levels correspond to flickers which are generated by difference of pixel voltage in odd and even frame. And we simulated repetitively the compensated image by our block diagram for reduction flicker. Consequently, we confirmed flickers have been decreased more than 87%. Furthermore, our method provides visualization and valid prediction for improvement of TFT-LCD panel

1. Objectives and Background

LCD sizes are increasing to compete with other flat panel displays and to satisfy customer requirements. As the size of panel get larger, it is much more difficult to achieve uniform panel quality. Namely, there are many technical issues to be resolved such as flicker, short selected row-line time, gray scale error, cross-talk, RC delay, and so forth. Flicker of them, especially, is a key panel quality parameter. This paper presents a method to minimize flicker as well as gray scale errors automatically across the entire panel by using a compensation of the gray scale level of image.

2. LCD flicker

In TFT-LCD inversion driving method, the column data are driven alternately to positive and negative polarities such as odd and even frame. The absolute value of each polarity should appear equal because the two polarities express the same pixel. But, the parasitic capacitance and resistance between the signal lines and electrode can cause kickback voltage or unstable common voltage. That is, the charged pixel voltage in odd and even frame is not same exactly. These differences in odd and even frame cause fluctuating luminance that appears as flicker. Therefore, the TFT-LCD manufacturing company has taken up the dot or column on behalf of frame inversion method in TFT-LCD inversion driving method. Because it is the dot or column inversion method nearly is not influenced by parasitic parameters between signal lines and pixel electrodes. Contrastively, the parasitic parameters have an effect on charging pixel voltage in frame inversion method. But, the power consumption is much lower than dot or column inversion method. If flicker is removed in frame inversion method, the effect value of it will be maximized. Therefore, our research proposed method to minimize flicker as well as gray scale error in frame inversion driving method.

3. The simulation method to minimize LCD flicker

In order to figure out the influence of the parasitic parameters on the image performance of the TFT-LCD panel, for instance, grey-scale errors as well as flickers, we propose a simulation method with feedback structure. Figure 1 is shown a schematic block diagram demonstrating a simulation procedure used in reduction of flicker as well as gray scale error. To simulation for full TFT-LCD panel with an equivalent circuit, we need to take values for TFT parameters, resistance, capacitance, and optic characteristics including V-T curve and gamma curve of one pixel according to LCDs mode. Those parameters, V-T curve and gamma curve were taken through numerical simulation of a TFT-LCD.

The gray level voltages of input image are extracted for a particular image (SVGA 800×600), are obtained through V-T curve and gamma curve. Now a kickback voltage of a pixel is calculated from any equivalent circuit. We simulated the portion of image, with 4by3 pixel arrays, for considering the parasitic parameters between adjacent signal lines and pixel electrodes. Figure 2(a) and (b) show a kickback voltage in odd and even frame in terms of red pixel. We considered that kickback voltages according to red, green and blue pixel are 0.5467, 0.544 and 0.5577 in odd frame and 0.4811, 0.4639 and 0.4731 in even frame respectively. Kickback voltages, actually, occur differently

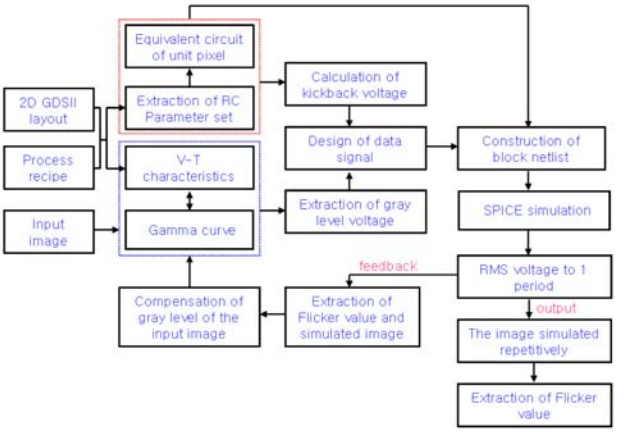
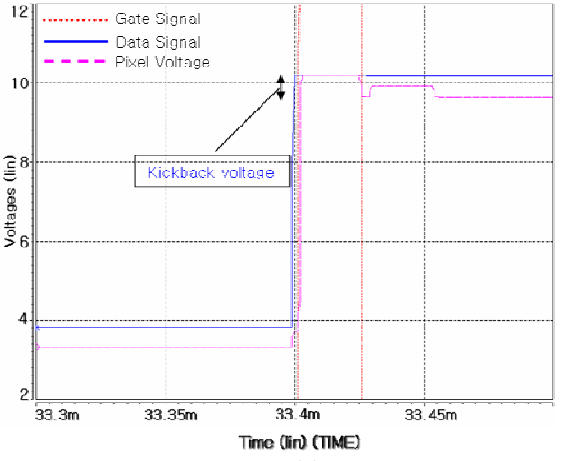
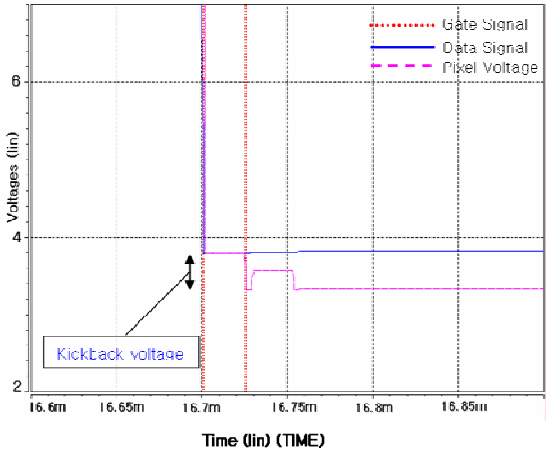


Fig. 1. Schematic block diagram for reduction flicker.



(a)



(b)

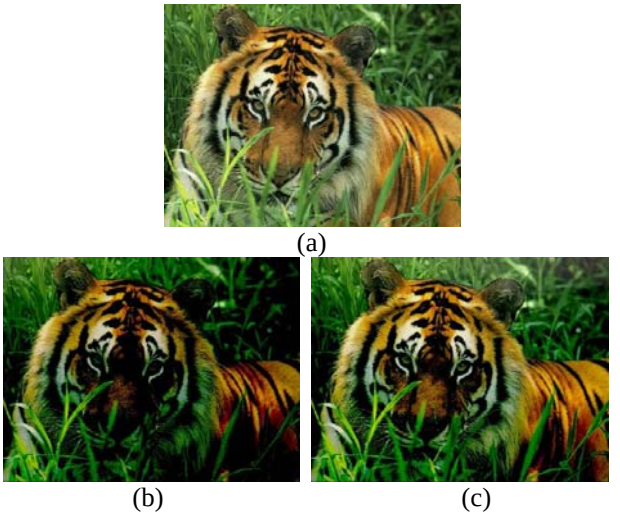
Fig. 2. (a) The kickback voltage in odd and (b) the kickback voltage in even frame in terms of red pixel.

in position of the image due to variation of the RC value according to the position of pixels on the screen. Although the kickback voltage is the dependence of position, we don't consider it, because the image for simulation is returned by our proposed block diagram with the compensated gray levels. The compensated gray levels correspond to the gray scale errors are generated by kickback and crosstalk according to pixel's position. And a data signals are designed for frame inversion from the gray level voltages and a kickback voltages. It should be also noted that the pulse width of gate and data signal is determined by the size of the panel as well as the signal frequency. It is assumed that widths of gate pulse and one data signal are 26.95 and 23.03considering RC delay and rising and falling time respectively.1) And the gate voltage ranges from -6 to 30V while the data voltage varies between 0 and 12.45V. And Common voltage was set 5.5V. Finally, a SPICE net-list about image is constructed for the whole block for image simulation by repeating the equivalent circuit and taking the parasitic resistances and capacitances along the bus line for gate and data signals. The net-list is made up gate, data signal, TFTs and parasitic parameters in terms of the bus line for gate and data signals. However, to simulate the net-list for entire panel, an enormous CPU times as well as huge memory is required. Therefore, we divided it into 600 such as the height of image to overcome the problem. As a result, we constructed 600 net-list for the SPICE simulation with equivalent circuits of pixel arrays, which corresponds to one gate line, and lumped RC model for data lines. The pixel is an MVA cell with a pixel size of micrometers. Especially, for LC capacitors and TFT, voltage-dependent model and a level 40 HP (Hewlett-Packard) a-Si model are used, respectively.2) And the root-mean-squared (RMS) value of a pixel voltage is obtained and then converted to an image data through the mapping of V-T and gamma curve.

4. Results and discussion

As a result of the first simulation, fig. 3(a), (b) and (c) show the original image, the simulated images in odd and even frame respectively.

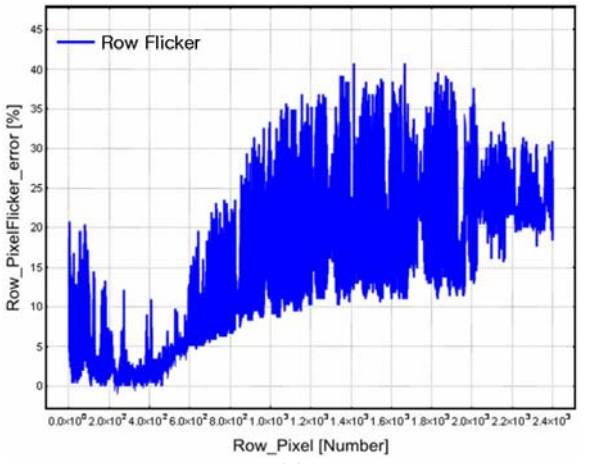
And fig. 4(a) shows that differences of luminance between odd and even frame along the first row line. The differences represent flicker. On average, the flicker error is 16.87 %. Figure 4(b) shows flicker along 800th column line. The flicker errors according to Red, Green and Blue pixel are 1.69%, 2.73% and 1.54% respectively. As shown the fig. 4(a), as the number of pixels is increased, flicker is larger because a pixel voltage is affected by signal line delay and parasitic parameter.3) That is, it represents that a pixel voltage is affected by signal line resistance and kickback voltage which is generated by parasitic parameters. The kickback voltage is solved by eq.(1). As shown eq. (1), the parasitic parameters between signal lines and pixel electrodes have an effect on kickback voltage.



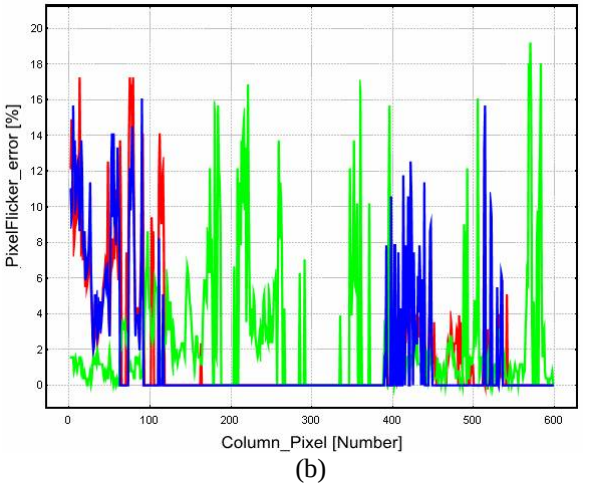
(a)

(b) (c)

Fig. 3. (a) Original image, (b) the first simulated image in odd frame and (c) the first simulated image in even frame.



(a)



(b)

Fig. 4. (a) Flickers in first row and (b) flickers in 800th column line.

As shown the fig. 4(a), as the number of pixels is increased, flicker is larger because a pixel voltage is affected by signal line delay and parasitic parameter.3) That is, it represents that a pixel voltage is affected by signal line resistance and kickback voltage which is generated by parasitic parameters. The kickback voltage is solved by eq.(1). As shown eq. (1), the parasitic parameters between signal lines and pixel electrodes have an effect on kickback voltage.

$$\Delta V = \Delta V' + \Delta V_{PG1} + \Delta V_{PG2} + \Delta V_{PD1} + \Delta V_{PD2} \quad (1)$$

In eq.(1), is kickback voltage by TFTs, and are kickback voltages between the adjacent left and right gate line respectively. and are kickback voltages between the adjacent upper and lower data lines. We paid attention to the above-mentioned fact carefully. If data signals are changed lightly and the others, for instance, gate signal, gate and data resistance and so on, are fixed, the flicker will be decreased. Therefore, to reduce the flicker and the gray scale error, we simulated repetitively the original image by our proposed simulation method with feedback structure. The meaning of repeatable simulation is to vary the data signal. The variation of data signal corresponds to the compensated gray scale level. Therefore, we compensated the data signal of original image. The compensated quantity corresponds to the difference of gray level voltage between odd and even frame. The compensated gray level voltage is solved by equation the following equations.

$$DropVol[0] = |OrVoltage - SiVol[0]| \quad (2\text{-}1)$$

$$DropVol[1] = |OrVoltage - SiVol[1]| \quad (2\text{-}2)$$

$$cVoltage[0] = DropVol[0] \pm OrVoltage \quad (3\text{-}1)$$

$$cVoltage[1] = DropVol[1] \pm OrVoltage \quad (3\text{-}2)$$

OrVoltage is the gray level voltage of original image, SiVol[0] and SiVol[1] are gray level voltages of the simulated image, DropVol[0] and DropVol[1] are differences of gray level voltages between original image and simulated image and cVoltage[0] and cVoltage[1] are the compensated gray level voltages in odd and even frame respectively. Then, the compensated gray level voltages are converted to gray scale level. Figure 5(a) and (b) show the compensated image in odd and even frame respectively.

Naturally, when the data signals are changed, the parasitic parameters also are changed according to data voltages. But compensated gray level voltages cover enough the changed kickback voltage Also, in our schematic block diagram with feedback, only variable which has an effect on flicker is the difference of data signal. The others unchanged, because the image simulation is performed repetitively through feedback structure.

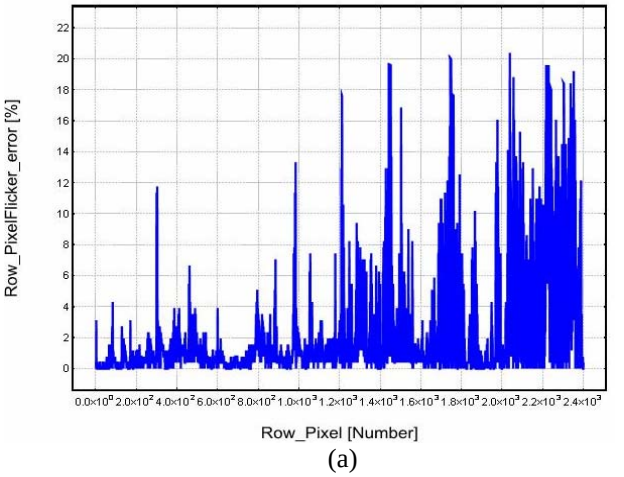
(a) (b)

Fig. 5. (a) Compensated image in odd frame and (b) compensated image in even frame

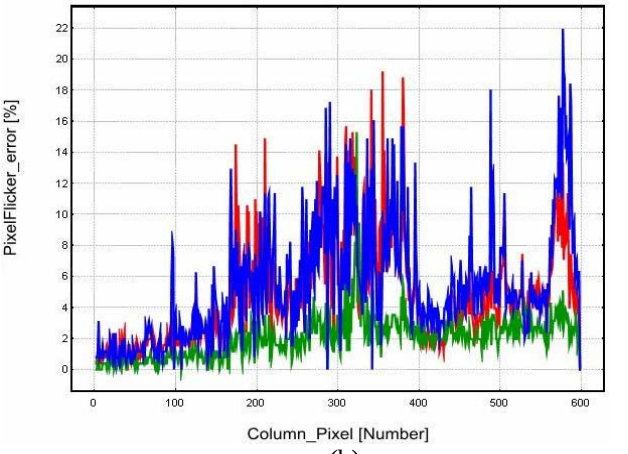
And the variation data signal is within the range of the maximum 0.1v and 0.2V in odd and even frame respectively. So, the influence of variation of the data signal also is very small. Consequently, flicker is decreased. As a result of the second simulation, fig. 6(a) and (b) show the simulated images in odd and even frame respectively. And fig. 7(a) shows flicker along the first row line. Flicker error is 2.19%. Flicker error along the first row line decrease 14.68% than flicker error of the first simulation. 7(b) shows flicker along 800th column line. On average, flickers along 800th column line increased than flicker errors of the first simulation. But, it is meaningless, because gray scale error is very large. On the contrary, in second simulation, the gray scale errors of odd and even frame decreased as shown table 1.

(a) (b)

Fig. 5. (a) The second simulated image in odd and (b) the second simulated image in even frame



(a)



(b)

Fig. 5. (a) Flickers in first row line and (b) flickers in 800th column line.

Therefore, through our proposed method, we confirm that flicker as well as gray scale errors can be minimized by the compensation of gray scale level. Furthermore, our simulation method can observe the gray scale errors, flickers and signal delay which influence to quality of TFT-LCD.

4. Conclusion

We presented a novel method to minimize flicker and gray scale error automatically across the entire panel by using a compensation of the gray scale level of image. Electrical characteristics for SVGA(800*600 of resolution) LCD panel have been simulated by considering parasitic parameters induced by signal lines. Especially, we observed flickers from the repetitively simulated image. And flickers and gray scale errors were decreased by our proposed simulation method with feedback structure.

5. Acknowledgment

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6. References

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