Field Emission Display with Design Elements for Control of Uniformity, Color Purity, Luminance, and Invisible Spacers.

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Abstract

A solution for carbon nanotube based field emission displays has been designed and built. The solution makes use of structure layout to control electron beam trajectories, uniformity by use of ballasting, emission anomalies eliminated by selective carbon nanotube growth and invisible spacers to maintain the vacuum gap.

1. Introduction

The flat panel display market has seen rapid growth in recent years. Liquid Crystal Displays have shown a remarkable ability to continue to expand into larger formats and bring prices down while adding complexity. Plasma and projection technologies for large area displays continue to advance to remain competitive in performance and price. As these technologies continue to improve they are often judged against CRT units for brightness, color purity, uniformity, and lifetime. The distinct advantage of CRT's is they do not compete in the large diagonal sizes beyond about 42". In this paper we show results which do not have the size limitation of CRT tubes and are less costly to produce than large LCD, Plasma and Projection display technologies.

We avoid adding cost by avoiding adding complexity. A conventional focusing grid is avoided by designing the device cathode and gate structures to act as a focusing grid, producing good color purity and efficiency. By using ballast resistance we control the emission current to each emitter pad in the display and produce a desirable short and long range luminance uniformity. The selective growth of carbon nanotube emitters is obtained by use of Hot Filament Chemical Vapor Deposition which allows us to avoid the activation required for nanotube paste technology as well as the associated defects. Understanding spacer charging provided us with a solution to maintain invisible spacers in a field emission display. With fewer processing steps than other flat panel display technologies, CNT FED's will require less capital investment and less fabrication cost.

2. Design and fabrication

The Carbon Nanotube (CNT) Field Emission Display (FED) is essentially a thin flat CRT. Because the viewer sees a flat plate (anode) with phosphor luminescing it has the same viewing experience as the CRT for high luminance, large viewing angle and high efficiency.

We have fabricated CNT FED's with a pixel size of 726um^2 which is designed for a 42" diagonal HDTV application with the actual size of the display we fabricated being 4.6" diagonal. Figure 1 shows a schematic view of a completed display. The anode uses P22 phosphors. The spacers are made of an insulating material and maintain a 1.7mm gap between the anode and the emitter plate.

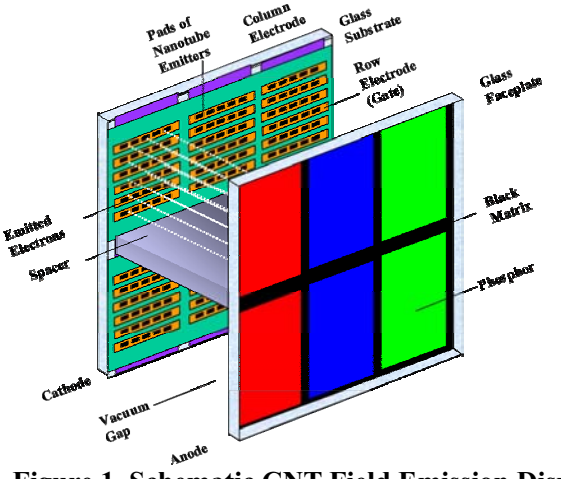

Figure 1. Schematic CNT Field Emission Display

The emitter plate or cathode is fabricated directly on display glass to match the anode glass and allow frit sealing of the two plates. The cathode metal is deposited and patterned. The layout of this metal pattern is such that it creates a trench opening which is where the carbon nanotubes will be located. The orientation of the trench is such that the longer edge of the trench is in the direction of the adjacent colors on the anode.

Next a resistive material is deposited over the cathode metal to create the emitter ballast. The resistance of the ballast is controlled by the type of film deposited, the film thickness and the distance from the cathode conductor to the catalyst pad.

The gate dielectric film thickness is set to a value which is nearly equal to the length of the carbon nanotubes grown on the emitter plate. The gate conductor is then deposited onto the gate dielectric and both layers are patterned. The gate trench has the same orientation as the cathode trench. We control the electron trajectory in the direction of different colored phosphors (X) where beam spread causes color error. In the direction where the color is not different we have added space reserved for periodic spacers (Y). With this orientation in mind we designed the subpixel emitter structure to create an electric field in mainly the Z direction. Since the X directed gate field exists only very close to the nanotube tip there is neither electron acceleration or deceleration in the X direction due to the cathode field. The anode field collimates the X-Z directed velocities in the Z direction. Figure 2 shows a model of the electrostatic potential in the area where nanotubes are located.

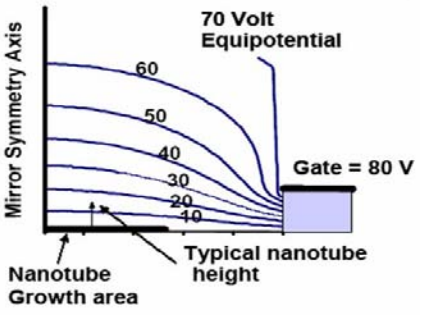

Figure 2. Electrostatic Potential Nanotube Region

The catalyst pads are then defined in the trenches created in the cathode conductor and the gate dielectric and gate conductor. As can be seen in figure 3 of the completed emitter plate the catalyst pads and gate conductor are easily visible. The reference of the view shown is through the anode plate looking directly toward the emitter plate. The ballast length would be from the edge of the catalyst pad to the edge of the cathode conductor which is obstructed by the gate conductor.

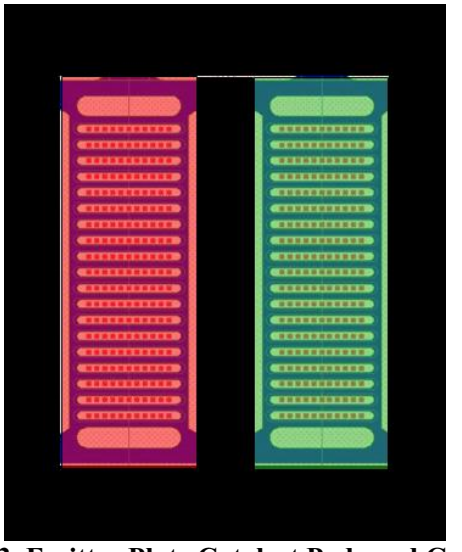

Figure 3. Emitter Plate Catalyst Pads and Gate Structure

Carbon nanotubes are then selectively grown by Hot Filament Chemical Vapor Deposition (HF-CVD) on the catalyst pads. By using HF-CVD we use a process which can maintain the emitter plate temperature below 600°C while having a sufficient temperature to grow carbon nanotubes, significantly higher than 600°C. By controlling the process conditions of the HF-CVD process we can control the density, number of walls and length of the nanotubes. Controlling these factors is critical to the operation of the device as they impact emission current density at a given extraction field potential. Control of the density and geometries of the nanotubes is important as they impact device design such as ballast resistance, gate dielectric thickness, and gate operating voltage.

Vacuum packages are fabricated by frit sealing the anode and emitter plates together. A hole is drilled into the emitter plate and a getter house and pinch off tube are fritted over the hole. A glass frame is fabricated and frit is applied to both sides which will form a seal to the emitter and anode plates. Spacers are then affixed to the anode plate. The emitter plate, frame and anode are placed into a fixture and aligned. The fixture is placed into an oven where the temperature is elevated in a controlled environment and the glass plates and frame are fritted together. In another step the pinch off tube is

attached to a vacuum pump and the package is baked and pumped to a low pressure. During this time the getter is flashed and the pinch off tube is sealed. A view of a functioning display with the getter house and pinch off tube visible is shown in figure 4.

Figure 4. View of CNT FED with Pinch Off Tube and 50% Neutral Density Filter

3. Results and discussion

Due to the hundreds of electron sources per subpixel in our nanotube display we must control slight differences in β (field enhancement factors) of the nanotubes.[1] We employed a ballast resistor for each emitter pad to maintain a short range uniformity variation to less than 4%, the detectable limit for a viewer. Electron emission current is exponentially dependent of the height to radius (h/r) ratio of the nanotube emitters, therefore as the h/r ratio varies so does the uniformity.

We used both the HF-CVD process parameters and the ballast resistance to minimize luminance variation in the carbon nanotube field emission display. The HF-CVD process is used to improve uniformity by setting the processing parameters to grow predominately the desired h/r nanotubes in a preferred density. The HF-CVD process can be tuned to grow a high yield of a certain h/r nanotube however, it still produces nanotubes in a distribution so high values of h/r are always present and must be accounted for. Our use of ballast resistance for each emitter pad limits the current of high h/r nanotubes, truncating the high end of the h/r curve. While higher ballast resistance values have shown improved uniformity they can limit emission current if the resistance value is too high, in short the optimal ballast resistor value will provide a short range non-uniformity of less than 4% and no more. Further increases in ballast resistance will decrease emission current density and the efficiency of the device.

A model to analyze the factors of the ballast resistor network, the number of ballasted pads in a subpixel and the overall number of nanotubes in a subpixel was created[2]. The model populates a section of the cathode with nanotubes from an h/r distribution input parameter. Other variable parameters include ballast resistance, the number of pads per subpixel and the number of nanotubes per pad. The model computes the current from each nanotube in the array as a function of gate and anode voltages and calculates the IV curve, the uniformity and numerous statistics. The model is in good agreement with the IV curves and uniformity values we measure.

We calculate that as the density of nanotubes increases the non-uniformity decreases. And in practice we see this is the case. We also see there is an upper limit to the density of nanotubes before electric field shielding begins to reduce the emission current. Using the HF-CVD process parameters we have grown nanotube densities which produce emitter current densities from 0.2mA/cm^2 to 5.0mA/cm^2. Without the use of filters on the anode plate we can produce luminance values for the entire display to above 1,000cd at Vg=85V and Va=5.5kV

Color purity is maintained by control of electron beam trajectory. Beam size is the result of electron trajectory and is a function of gate voltage (Vg), anode voltage (Va) and cathode to anode spacing. Device measurements show a minimal dependence of the sub-pixel beam size with changes in Vg, figure 5, which is a result of the device layout discussed previously which minimizes the forces on electrons in the X and Y directions. As Va increases the beam size decreases, figure 6. The beam size increases as the anode-emitter plate spacing increases, figure 7. With the impact from these sources on the beam size understood the display is designed accordingly.

Spacers in FED's can be bombarded by both primary electrons (PE) from the emission source and backscattered electrons (BSE) from the anode plate[3]. We have already discussed the method we use in the cathode design to minimize the impact of PE on the spacers. The control of BSEs cannot be controlled by the emitter plate design as the source of these electrons is outside the influence of the emitter plate. With a low number of PE's striking the spacer we focus on the

BSE's as the source of spacer charging.

As BSE's impact the spacer a charge accumulates on the spacer and begins to influence the trajectory of the PE's. For this to occur we assume that as the electrons impact the spacer the secondary electron emission coefficient (SEC) is >1. As this cycle continues the PE trajectory is influenced to a greater degree and eventually the PE will impact the spacers prior to impacting the anode which usually results in an arc.

Spacers become visible when the charge on the spacer has reached a level that they have a significant affect on the trajectory of the PE's which are being accelerated by the anode field. We also know the anode field can influence the time before the spacer becomes visible. Simply stated, increased anode voltage increases the time before sufficient spacer charging takes place for a spacer to become visible. We have developed a method which can alleviate the spacer charge and prevent the spacers in the FED from reaching the point where significant PE trajectory deviation occurs. Due to limitations on space here a future paper will be presented on the subject.

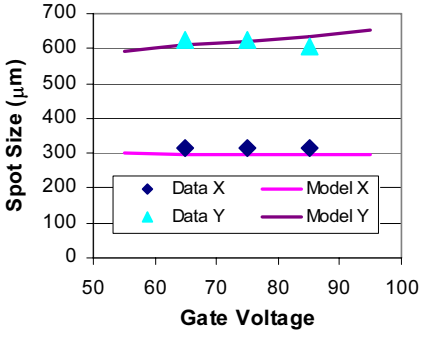

Fig. 5. Beam Size Vs Gate Voltage

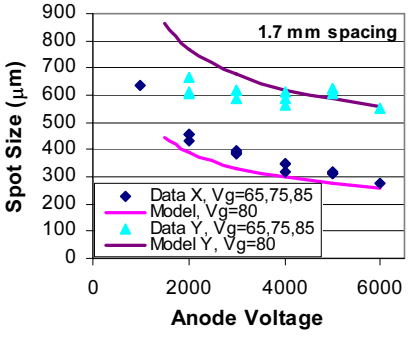

Fig. 6. Beam Size Vs Anode Voltage

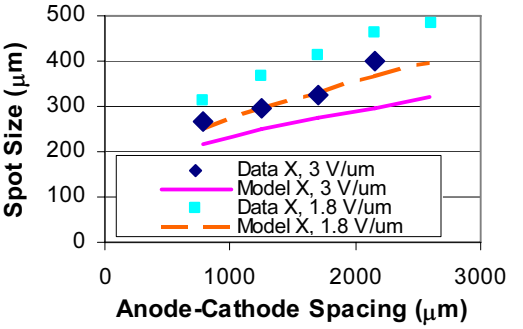

Fig. 7. Beam Size Vs Anode to Cathode Gap

4. Summary

We have designed and built a carbon nanotube field emission display prototype with minimal processing steps to produce a display solution for large area flat panel displays. The rather than add complexity by using TFT type control circuits or conventional focusing grids the display is designed to have the functions by using existing layers to complete multiple tasks and eliminate the added cost associated with the added layers and complexity. The prototype built is competitive with CRT, LCD, PDP and Projection displays with respect to luminance, uniformity, color purity, viewing angle and efficiency.

5. Acknowledgements

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6. References

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