Polysilicon Thin Film Transistors on spin-coated Polyimide layer for flexible electronics

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Abstract

We developed a non self-aligned poly-silicon TFTs fabrication process at two different temperatures on spin-coated polyimide layer above Si-wafer. After TFTs fabrication, the polyimide layer was mechanically released from the Si-wafer and the devices characteristics were compared. In addition self-heating and hot-carrier induced instabilities were analysed.

1. Introduction

Flexible panels can be now made by optimizing low-temperature process polysilicon (LTPS) thin film transistors (TFTs) fabricated directly on polymer substrate. Flexible electronics offers many advantages over rigid backplane, such as lower production cost, lightness and robustness [1]. The LTPS TFTs fabrication process, in fact, is becoming totally compatible with new polymeric materials that have higher glass transition temperatures, low surface roughness and low Coefficient of Thermal Expansion (CTE) as polyarylite (PAR) and polyimide (PI) films [2]. However some problems are still present in the fabrication process such as difficulties of polymer substrate handling, the need to protect polymer from external chemical agents and thermal stress that can induce polymer substrate shrinkage. In order to overcome these problems, excimer laser crystallization technique can be used, since it allows, at the same time, a partial dehydrogenation of the amorphous silicon film and the melting of the precursor layer, minimizing the thermal budget on the polymer substrate. Furthermore the high density plasma and the low deposition pressure, achieved in the ECR and ICP CVD techniques, make possible the deposition of low temperature stoichiometric SiO_2 films with good electrical properties [3, 4]. In order to eliminate polymer shrinkage during the fabrication process and overcame the problem of substrate handling, a new a-Si TFTs fabrication method on polyimide layer has been recently proposed by Philips Res. Lab. In this procedure, PI is spin-coated onto glass substrate and laser released after device fabrication (EPLaR) [5]. In this work we show that it is possible to fabricate low-temperature poly-Si TFTs on PI layers, using a similar process where the PI substrate is mechanically separated from a Si-wafer carrier allowing the use of standard semiconductor equipments. In particular, we compared electrical characteristics of LTPS TFTs fabricated at two different maximum process temperatures (350°C and 400°C respectively). We analysed also electrical stability in both self-heating and hot-carrier regimes.

2. Experimental

We start fabrication process depositing PI spin-coated onto 3'' thermally oxidized Si-wafer. After curing at a maximum temperature respectively of 350° C and 400°C, we achieved a 8 µm thick PI film. The cured polyimide offers a low CTE of about 3 ppm/°C, which closely matches that of silicon substrate. This low thermal expansion does not produce significant mechanical stress upon heating and cooling, avoiding cracking of the upper layers during deposition and laser annealing.

Before starting deposition of active layers, we grow on polyimide a silicon nitride film at 300°C, 200 nm thick, by using a dual frequency plasma enhanced chemical vapour deposition (PECVD) system, from a mixture of SiH_4, NH_3, N_2 and He gases. Subsequently, a silicon oxide film of about 250 nm is deposited at 200°C, by an electron cyclotron resonance ECR-PECVD system, in order to obtain a buffer layer with a low hydrogen content, avoiding possible hydrogen desorption in the active layer during the laser

crystallization step. After the deposition of the two different capping layers on polyimide, a film of hydrogenated amorphous silicon (a-Si:H), 100 nm thick, is deposited by PECVD at a temperature of 300°C. Then, a highly doped a-Si:H PECVD layer (25 nm thick) is deposited by PECVD at a low temperature, using a SiH_4+PH_3 (1%) gas mixture. According to a conventional non self-aligned process, source and drain regions were defined by photolithography, removing the n^+ film from the channel regions using a selective wet etching [6]. Subsequently, the samples were furnace-annealed respectively at 350°C and 400°C in N_2 atmosphere for 16 hours, to partially remove hydrogen from amorphous silicon layer. Then the samples were irradiated by excimer laser using a gradual energy laser beam profile, in order to promote hydrogen evolution remained in the a-Si layer. In this step the channel region was transformed into polysilicon and the dopant, present in the source and drain regions, was also activated. The sample dehydrogenated at higher temperature was irradiated at a maximum laser energy of about 400mJ/cm^2, in order to avoid material damages due to rapid hydrogen evolution obtaining a polysilicon layer with an average grains size of about 250nm (see Fig. 1). For the lower process temperature sample, the maximum energy density we could use was 300mJ/cm^2, since higher energies caused damage of the polysilicon film, and the average grain size was in this case of 100nm, as observed in the AFM analysis (Fig.1a). After definition of the active layer island, the gate oxide was deposited (130 nm thick) at room temperature by ECR-PECVD from a SiH_4+O_2+He gas mixture [3]. Then, via-holes were opened by wet etching and Aluminum+1%Si was deposited, to form source, drain and gate electrodes. Finally, to passivate Si-dangling bonds at the semiconductor-insulator interface, post-annealing treatments at 350°C in N_2 atmosphere for 30 minutes was performed on both samples. When the device fabrication was completed, the PI layer was mechanically released from the rigid carrier, which can be re-used for a new fabrication process (see Fig. 2). It could be noted that, due to the low mechanical stress of the deposited films, no bending problems of the freestanding PI film were observed.

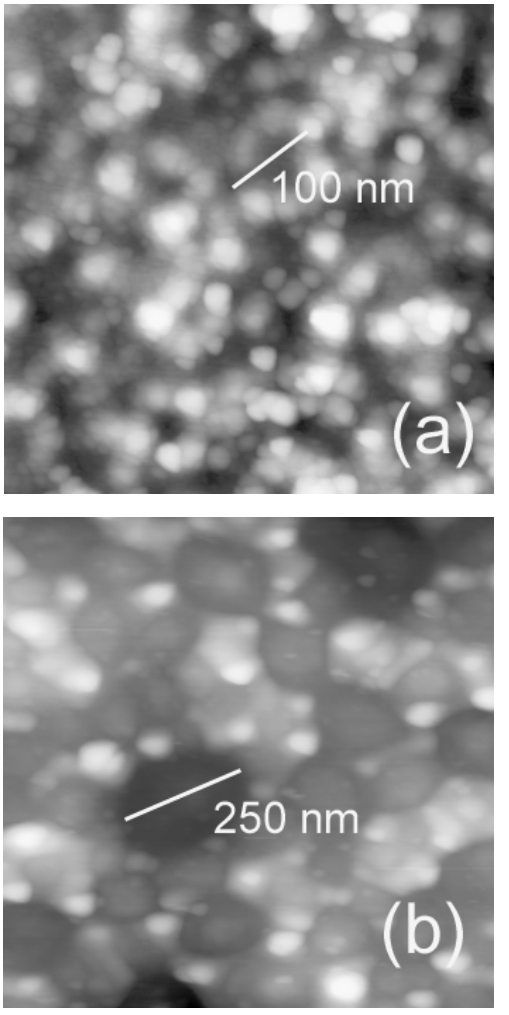

Fig. 1: AFM analysis of Polysilicon grain sizes after excimer laser crystallization for two different dehydrogenation temperatures (a) 350°C (b) 400°C.

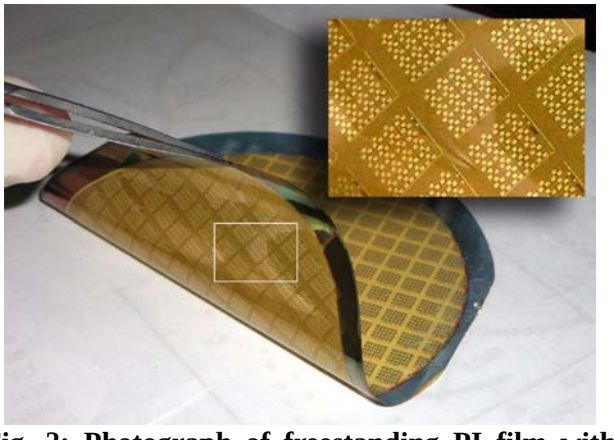

Fig. 2: Photograph of freestanding PI film with LTPS TFTs, after mechanical release.

3. Electrical characterization

We analysed the transfer and the output characteristics of the poly-Si TFTs on PI, observing good performances for both samples processed at two different temperatures. The TFTs electrical characteristics were compared as shown in Fig. 3a,b. We measured leakage currents below 10 pA, Ion/Ioff current ratios greater than 10^6, and threshold voltage V_t=6-8 V for both samples. As can be seen, indeed the devices fabricated at higher temperature exhibit a greater mobility (70 cm^2/Vs) and lower subthreshold slope (0.9 V/dec) respect to the sample processed at 350°C that shows a mobility of 40 cm^2/Vs and subthreshold slope of 1.2 V/dec.

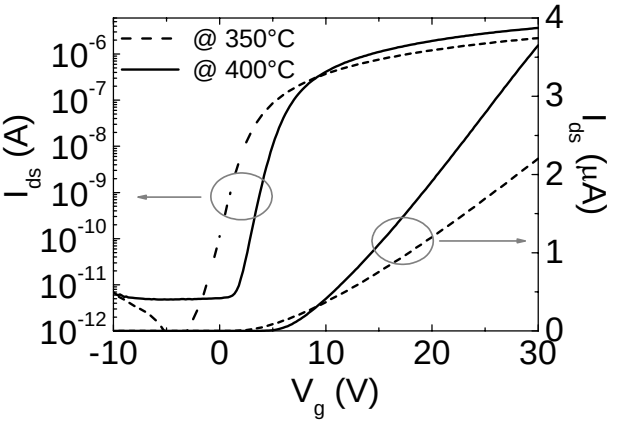

Fig. 3: Semilog and linear scale transfer characteristics for TFTs with maximum process temperatures of 350°C (dashed line) and 400°C (solid line).

We investigated the electrical stability of the devices, processed at the higher temperature (400°C), bias-stessing the poly-Si TFTs in self-heating regime and in the hot carrier regime. First we performed electrical stress experiments applying a V_g= 30 V and a V_{ds}= 15 V for 10^4s in order to induce appreciable Joule heating (about 7.5 mW) in a device with L=20 μm W=40 μm, with the TFTs still working in the linear regime. In fig.4 the transfer characteristics show a threshold voltage increase, a subthreshold slope degradation and a on-current reduction for increasing bias-stress times. Self-heating related instability seems to seriously affect the performances of the devices, worsening the transfer characteristics in a permanent way. In order to evaluate the temperature reached in the device, with the specified channel geometry, due to self-heating, we performed a bias stress simply increasing the temperature on the wafer at 120°C and

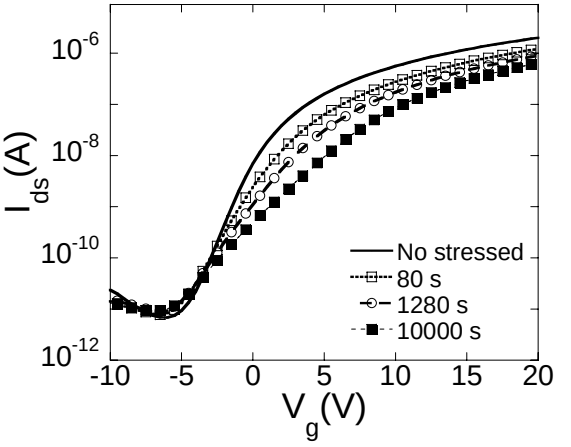

Fig. 4:Experimental transfer characteristics measured at different time of bias stress with V_{ds}=0.1 V. Bias stress conditions: V_g-V_t=25 V_{ds}=15 V.

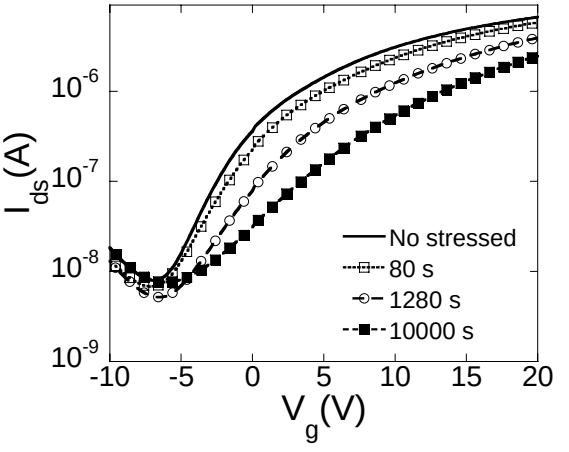

Fig. 5: Experimental transfer characteristics measured at different time of bias stress with V_{ds}=0.1 V at a temperature of 120°C. Bias stress conditions: V_g-V_t=25 V_{ds}=0 V.

increasing the temperature on the wafer at 120°C and applying, at the same time, a gate voltage V_g= 30 V and no drain bias along the channel (V_{ds}= 0 V) for 10^4s. As can be seen in fig.5, the instability behaviour is very similar to the effects observed in self-heating regime. This suggests that the temperature of the polysilicon active layer in self-heating regime is close to 120°C. Further investigations are needed to provide a more complete description of self-heating, however we can attribute the positive shift of V_t and the degradation in subthreshold slope to a combination of electron charge injection into the gate oxide and interface state generation [7]. The electrical stability of TFTs was also investigated in hot-carrier regime by applying prolonged bias-stress with V_g=V_t and high

V_{ds}. In Fig. 6a the transfer characteristics (at V_{ds}=0.1 V) measured during bias-stress performed at V_g=V_t=6 V and V_{ds}=15 V are shown. As can been seen an appreciable transconductance degradation occurs due to hot carrier effects: this can be attributed to the formation of interface states close to the drain junction were the electric field is maximum.

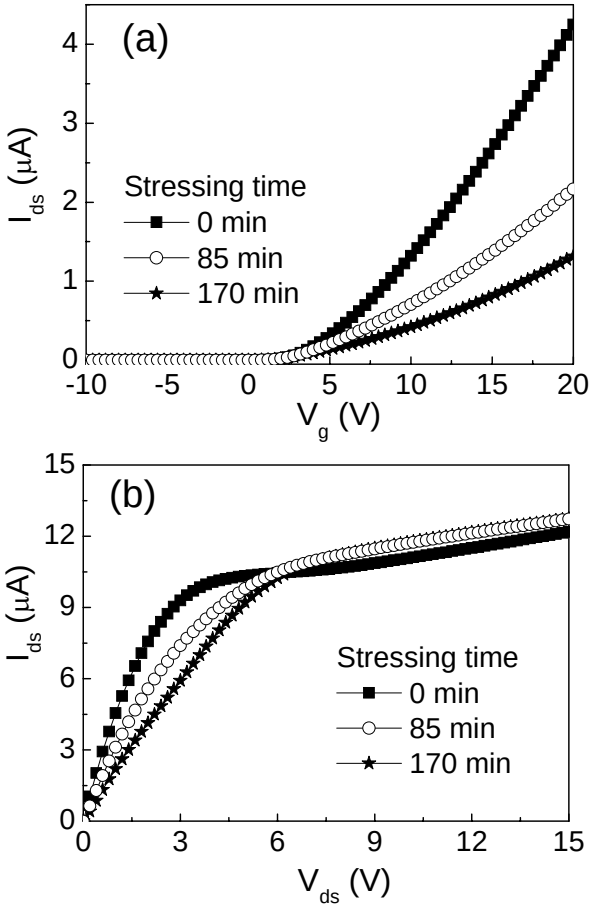

Fig. 6: (a) Transfer electrical characteristics for a device with L=10 μm W=40 μm measured at V_{ds}=0.1 V for increasing stressing times at V_g=V_t=6 V and V_{ds}=15 V. (b) Output electrical characteristics measured at increasing stressing times and same bias stress condition.

By referring to Fig. 6b a common cross point (around V_{ds}=6 V) is evident that distinguishes two main regions: the low V_{ds} region, where the drain current after bias-stressing is considerably lower than the initial condition and high V_{ds} region, where the drain current exceeds the one before stressing. The I_{ds} reduction observed in the first region can be explained by considering that the damaged region (related to the presence of interface states) acts as a parasitic resistance in series with the undamaged channel region. Moreover, the observed I_{ds} increase, after bias-stressing, that occurs at high V_{ds}, can be attributed to an increase in the impact ionization rate due to the presence of interface states in the damaged region.

4. Summary

We fabricated poly-Si TFTs on PI layer spin-coated on a Si wafer used as rigid carrier at two different process temperatures 350°C and 400°C. The sample processed at higher temperature allowed to increase the maximum laser energy (400 mJ/cm^2) obtaining a larger grain size (of about 250 nm) respect to the process at 350°C (100 nm) as confirmed by the AFM analysis. The devices fabricated at higher temperature exhibited a greater mobility (70 cm^2/Vs) respect to lower process temperature sample (40 cm^2/Vs). In addition, subthreshold slope improves from 1.2 V/dec to 0.9 V/dec. We investigated the electrical stability of the devices, processed at 400°C, bias-stessing the poly-Si TFTs in both self-heating and hot-carrier regimes.

Acknowledgements

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5. References

1. S. D. Theiss, P. G. Carey, P. M. Smith, P. Wickboldt, T. W. Sigmon, Y. J. Tung, and T.-J. King, *IEDM Tech. Dig.*, pp. 257–260, (1998).
2. N. D. Young, M. J. Trainor, S.-Y. Yoon, D. J. McCulloch, R. W. Wilks, A. Pearson, S. Godfrey, P. W. Green, S. Roosendaal, and E. Hallworth, *Proc. Materials Research Soc. Symp.*, **769,** (2003) H2.1.
3. L. Maiolo, A. Pecora, G. Fortunato and N. D. Young, *J. Vac. Sci. Technol. A* **24**(2) pp.280-285, (2006).
4. J. S. Jung, J. Y. Kwon, Y. S. Park, D. Y. Kim, H. S. Cho, K. B. Park, X. Wenxu, H. Lim, H. Yin and T. Nouguchi, *Proc. AM-LCD* 255-256, (2004).
5. I. French et al., *SID 2005 Boston Conference Proceedings*, pp.634-637, (2005).
6. M. Cuscunà, A. Bonfiglietti, R. Carluccio, L. Mariucci, F. Mecarini, A. Pecora, M. Stanizzi, A. Valletta and G. Fortunato, *Solid-State Electronics*, **46**, 9 (2002).
7. G. Fortunato, P. Gaucci, L. Mariucci, A. Pecora, A. Valletta, *IMID 2007 Digest*.