A substrate bias effect on the stability of a-Si:H TFT fabricated on a flexible metal substrate

Chang-Wook Han[1,2], Woo-Jin Nam[1], Chang-Dong Kim[1], Ki-Yong Kim[1], In Byeong Kang[1] , In-Jae Chung[1], and Min-Koo Han[2]

[1] LG.PHILIPS LCD R&D Center Anyang, Gyongki-do 431-080, Korea

TEL:82-31-450-7445, e-mail: hcw@lgphilips-lcd.com

[2] School of Electrical Engineering, Seoul National University, Seoul 151-742, Korea

Keywords : flexible, a-Si:H TFT, metal foil, substrate bias

Abstract

Hydrogenated amorphous silicon thin film transistors were fabricated on a flexible metal substrate. A negative voltage at a floated gate can be induced by a negative substrate bias through a capacitor between the substrate and gate electrode. This can recover the shifted-threshold voltage to an original value.

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs), which were fabricated on a flexible substrate, are good candidates for flexible active matrix organic light-emitting diodes (AMOLEDs) [1]. Flexible stainless-steel substrates are most promising candidates for use in flexible AMOLED displays because of their features of a small thickness and ruggedness. They are an excellent barrier against oxygen and moisture [2]. The a-Si:H TFTs represent a mature technology for use in low-cost and large displays. Furthermore, recent enhancements in OLED efficiency have provided a wider opportunity for a-Si:H TFTs to drive AMOLEDs.

However, it is well known that the stability of the a-Si:H TFT is rather poor as indicated by the threshold voltage shift (ΔV_{TH}) under bias temperature stress (BTS). In a conventional 2-TFT pixel circuit, the output current is sensitive to the ΔV_{TH} of the driving TFT. This leads to a degradation of the luminance of the OLED pixel over time. Several methods have been introduced to reduce the sensitivity of the current to ΔV_{TH}. They are the current-programmed circuit [3,4], voltage-programmed circuit [5], and reverse bias annealing methods [6]. In the reverse bias annealing method, ΔV_{TH} was reduced by a fraction time annealing. During the fraction time, a reverse bias was supplied to a gate electrode of a driving transistor, then ΔV_{TH} was suppressed. All of these methods need more than three TFTs and many bus lines for each pixel. These methods are too complicated in a driving scheme to achieve a highly reliable display.

When stainless-steel (SS) metal is used as a substrate, the surface of the SS should be planarized and insulated by dielectric materials, which make up what is called the passivation layer. The captive coupling between the display circuits and the SS substrate was considered for the design of displays by Hong et al [7]. The captive coupling from the SS substrate caused more data and scan line delay than in the glass substrate case. Therefore, the passivation layers preferred a larger thickness and a low dielectric constant to reduce the captive coupling. On the other hand, the SS substrate can be used as the common power. If a negative bias is applied to the SS substrate the captively coupled gate electrode is induced as a negative bias, that recovers the ΔV_{TH} of the a-Si:H TFT without additional complicated circuits.

In our work, we propose a substrate biased structure using capacitors between the gate electrodes and the SS substrate. This structure enables recovery from the threshold voltage shift of the a-Si:H TFT. In addition, we show the results of a potential simulation in which recovery of the drain current is realized by the negative bias at the substrate.

2. Experimental

We fabricated a-Si:H TFTs on a 76-μm-thick SS substrate. The root-mean-square (rms) roughness of

the SS substrate was 110 nm. A multi barrier as an initial surface passivation was coated on a SS substrate in order to reduce the surface roughness of the metal substrate. The multi barrier consisted of a several μm-thick low-dielectric constant polymer which showed a dielectric constant of about 3 and 200-nm-thick silicon nitride. The low-dielectric constant polymer was spin-coated and silicon nitride was deposited by plasma-enhanced chemical vapor deposition (PECVD). The rms of the SS substrate that was passivated with a multi barrier was 10 nm. The passivation layer also served as the mechanical bond between the TFT layers and the substrate. The structure of the a-Si:H TFTs was an inverted staggered-type structure which was fabricated by a conventional five-photomask process as shown in Fig. 1.

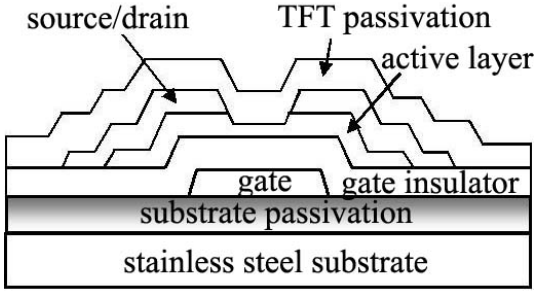

Fig. 1 Cross section of an inverted staggered-type TFT fabricated on a stainless-steel substrate.

3. Results and discussion

3.1 Substrate bias effect on the recovery of shifted threshold voltage in a single TFT

The SS substrate was passivated by dielectric materials in order to planarize the rough substrate. This passivation layer acted as a capacitor between the gate electrode and the SS substrate. When V_{DD} was grounded and the substrate was biased as a negative voltage during idle time, the floating gate electrode of the driving transistor was induced as a negative voltage by the passivation capacitor.

We simulated potentials of the TFT on the SS substrate when a drain electrode, which was connected to the V_{DD} line, was grounded and the substrate was negatively biased. The capacitances per unit area of the active and gate dielectric (C_1) and the passivation layer (C_2) were 12.7 and 2.4 nF·cm^{-2}, respectively. Although C_1 was larger than C_2, the area between the substrate and the gate electrode was usually much larger than that between the drain and

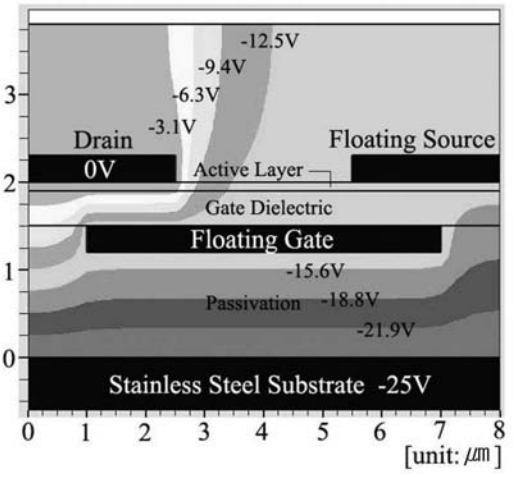

Fig. 2. Example of potential plot in simplified TFT structure when substrate is negatively biased and drain electrode is grounded.

gate electrodes. A large portion of the substrate voltage was induced by the floating gate electrode due to the larger capacitance of the gate electrode and the substrate. Fig. 2 shows an example of the potential plot in the simplified TFT structure when the substrate was negatively biased and the drain electrode was grounded. The gate-drain voltage (V_{GD}) was negative and the gate-source voltage (V_{GS}) was almost zero because the potential between the gate and source electrode was almost the same. Therefore, the threshold voltage can be shifted to the negative direction due to the extraction of the trapped charges by the negative V_{GD}. After the driving transistors were degraded, which meant a drain-current drop and a threshold voltage increase, the negative voltage at the substrate and grounded-V_{DD} lines during idle time enabled recovery of the degraded transistors.

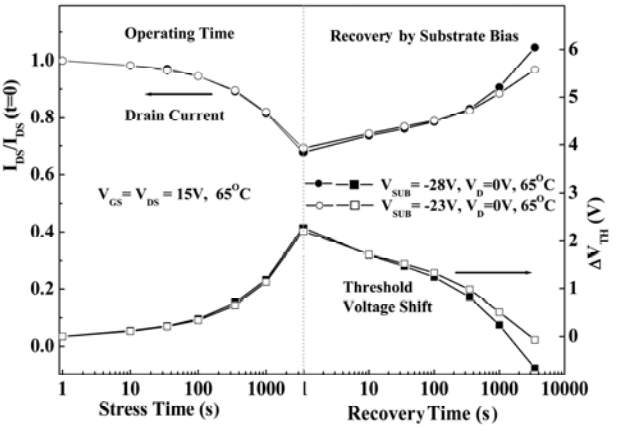

Fig. 3. I/I_o and ΔV_{TH} of a driving TFT as a function of stress and recovery time.

The recovery of the drain current and the negative shift of threshold voltage, as a function of the substrate bias, are shown in Fig. 3.

The V_{TH} of the TFT increased by 2.3 V and the drain-current decreased by 68 % of the initial value under a gate bias of +15 V and a drain bias of +15 V at 65 ^{o}C applied for 3,500 s. V_{TH} decreased by -2.3V and the drain-current recovered 97 % of its initial value when the substrate voltage was -23 V at 65 ^{o}C applied for 3,500 s.

3.2 Substrate bias effect on the recovery of shifted threshold voltage in a TFT array

If the substrate bias effect is applied to AMOLED displays, the pixel circuits with two transistors and one capacitor (2T1C) should be considered. Just before idle time, a constant V_{DATA}, for example 0 V, is required to set the initial voltage of the floating gate electrode of the driver TFT. Next, a negative select voltage is required to maintain the off state of the switch TFT during the idle time. During the idle time, V_{DD} should be grounded and V_{SUB} supplied a negative voltage to enable recovery of the degraded driver TFT. In the 2T1C circuit, the voltage of the floating gate (V_{FG}) will also be influenced by the storage capacitance (C_{ST}). After the driving transistors were degraded, which meant a drain-current drop and a threshold voltage increase, the negative voltage at the substrate and grounded-V_{DD} lines during idle time enabled recovery of the degraded transistors.

4 inch diagonal TFT array was designed for AMOLED display of which pixel circuit was 2T1C configuration. Fig. 4 shows pixel circuit considering parasitic and substrate capacitances.

Node A indicates the floating gate electrode of the driving TFT which will be induced negative bias by the negative substrate bias. The capacitance per unit area of planarization, SiNx/a-Si:H, and SiNx passivation is 2.4E-17, 1.27E-16, and 1.51E-16, respectively. The negative voltage which was induced at node A by substrate bias was verified by SPICE simulation. Before supplying a negative bias at the metal foil substrate, V_{DD} was set as 0 V. Data and scan line were applied 0 and -5 V, respectively, then both lines were cut off from electrical sources. The gate electrode of the driving TFT was floated. V_{SUB} swung from 0 to – 30 V then the floating gate electrode of the driving TFT was negatively biased. The level of voltage is defined as capacitance sharing among capacitances connected to the node A.

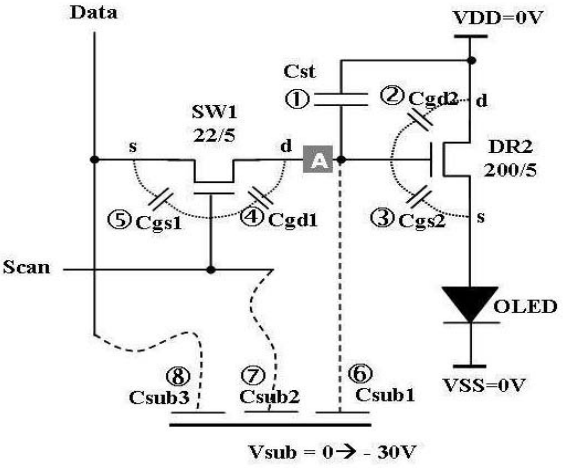

Fig. 4. Pixel circuit considering parasitic capacitances and substrate capacitances

The voltage of the node A can be calculated by a following relationship.

$$V_A = \frac{C_{sub1}}{C_{st} + C_{gd2} + C_{gs2} + C_{gd1} + C_{sub1}} \bullet V_{sub} \quad (1)$$

From Eq. (1), V_A was calculated as -7.8 V when V_{sub} was -30 V.

4 inch diagonal TFT array which had 320 x 3 x 240 pixels was fabricated for AMOLED display of which pixel circuit was 2T1C configuration. Fig. 5 shows a-Si:H TFT backplane fabricated on the SS substrate. This is designed for AMOLED display.

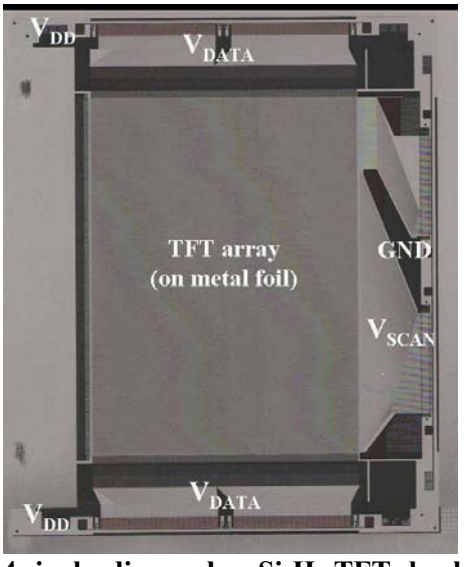

Fig. 5. 4 inch diagonal a-Si:H TFT backplane fabricated on the SS substrate. This is designed for AMOLED display.

The recovery of the drain current and the negative shift of threshold voltage, as a function of the substrate bias, are shown in Fig. 6. The size of driving TFT is W = 200 and L = 5 ㎛. The V_{TH} of the TFT increased by 0.95 V and the drain-current decreased by 83 % of the initial value under a gate bias of +15 V and a drain bias of +15 V at 65 °C applied for 3,500 s. V_{TH} decreased by -1.19 and 1.74 V and the drain-current recovered 111 and 154 % of its initial value when the substrate voltage was -25 and -30 V at 65 °C applied for 3,500 s, respectively.

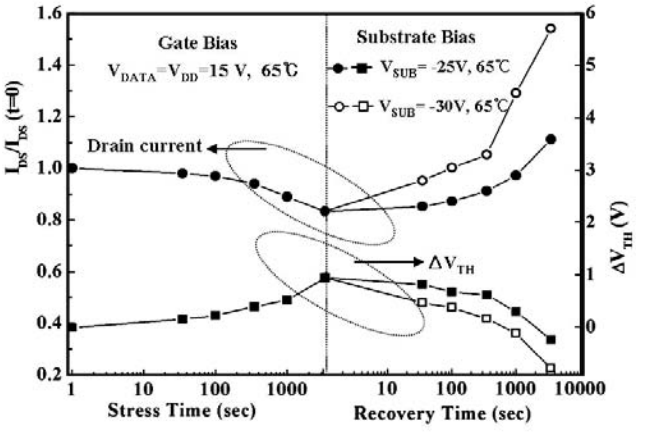

Fig. 6. Drain current and threshold voltage transition of a driving TFT as a function of stress and recovery time. V_{DATA} = V_{DD} = 15V is applied to the driving TFT at 65 ℃ for stress time and V_{SUB} = -25 and -30 V is applied to SS substrate at 65 ℃ for recovery time.

4. Summary

We have proposed a negative bias effect using the substrate bias without additional circuits to enable recovery of the degraded drain-current of a TFT which was fabricated on a stainless-steel substrate. The V_{TH} of TFT increased by 2.3 V and the drain-current decreased by 68 % of the initial value under a gate bias of +15 V and a drain bias of +15 V at 65 °C applied for 3,500 s. The V_{TH} decreased by -2.3 V and the drain current recovered by 97 % of its initial value when the substrate voltage was -23 V at 65 °C applied for 3,500 s. We also investigated the effects of negative substrate-bias in TFT array of which pixel was designed with 2T1C. When V_{DD} was grounded and the substrate was biased as a negative voltage during idle time, the floating gate electrode of the driving transistor was induced as a negative voltage by the dielectric capacitor. The V_{TH} of the TFT increased by 0.95 V and the drain-current decreased by 83 % of the initial value under a gate bias of +15 V and a drain bias of +15 V at 65 °C applied for 3,500 s. V_{TH} decreased by -1.19 and 1.74 V and the drain-current recovered 111 and 154 % of its initial value when the substrate voltage was -25 and -30 V at 65 °C applied for 3,500 s, respectively. The degraded drain current of the driving transistor can be recovered during the idle time by simply applying a negative substrate bias. The power consumption can be neglected during the idle time because no current flows.

5. References

1. C. C. Wu, S. D. Theiuss, G. Gu, M. H. Lu, J. C. Sturm, S. Wagner, and S. R. Forrest: IEEE Electron Device Lett. Vol. **18**, pp.609 (1997).
2. M. Wu, K. Pangal, J. C. Sturm, and S. Wagner: Appl. Phys. Lett. Vol. **75**, pp.2244 (1999).
3. Y. C. Lin, H. P. D. Shieh, and J. Kanicki: IEEE Trans. Electron Devices Vol. **52**, pp.1123 (2005)
4. S. J. Ashtiani, P. Servati, D. Striakhilev, and A. Nathan: IEEE Trans. Electron Devices **52**, pp.1514 (2005).
5. J. C. Goh, J. Jang, K. S. Cho, and C. K. Kim: IEEE Electron Device Lett. **24,** pp.583 (2003).
6. J. H. Lee, B. H. You, C. W. Han, K. S. Shin, and M. K. Han: SID Int. Sym. Dig. Tech. Pap. **36,** pp.228 (2005).
7. Y. T. Hong, G. Heiler, R. Kerr, A. Z. Kattamis, I. C. Cheng, and S. Wagner; SID Int. Sym. Dig. Tech. Pap. **37**, pp.1862 (2006).