4 inch QVGA AMOLED display driven by GaInZnO TFT

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Abstract

We demonstrated 4 inch QVGA AMOLED display driven by GaInZnO TFT. The structure of GaInZnO TFT is back channel etch (BCE) which is conventional structure for a-Si TFT. The electron mobility of GaInZnO TFT is 2.6 cm^2/Vs and Vt is 3.8V. It is thought that GaInZnO TFT could be backplane for AMOLED TV.

1. Introduction

For realizing AMOELD TV, one of the key obstacles is to fabricate uniform and reliable TFT array. In the case of a-Si TFT, it has uniform electrical characteristic over Gen 8 size, but Vt was changed during OLED driving. Even thought low temperature poly Si TFT shows stable electrical characteristics during OLED driving, it is not so easy to get uniformity at large area. GaInZnO TFT could be one of the candidates for backplane of AMOLED TV, because it is stable during current driving and it could be uniform because GaInZnO film has amorphous phase like a-Si film.[1,2] For not only AMOELD TV but also AMLCD TV, GaInZnO TFT has great advantage. It is higher electron mobility compared with that of a-Si TFT.[3~5] As TV size and resolution increases, turn-on-time of TFT decreases because RC delay and the number of gate line increase. In order to charge the capacitance within reduced turn-on-time of TFT, high electron mobility is required. In spite of such advantages of GaInZnO TFT, only a few GaInZnO TFT array was reported. In this paper, we tried to optimize the structure and process of GaInZnO TFT and fabricate AMOLED display.

2. Experimental

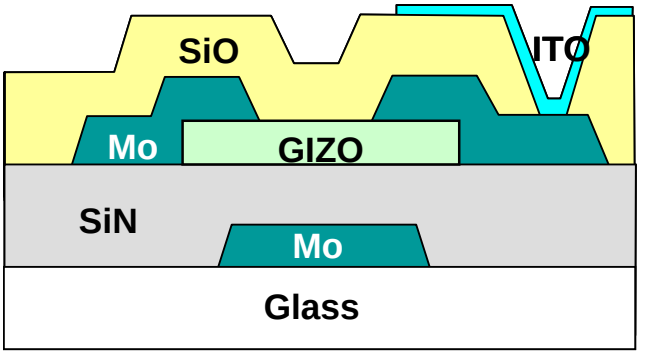

Fig. 1. Schematic diagram of GaInZnO TFT

Figure 1 shows the schematic diagram of GaInZnO TFT structure. The structure of GaInZnO TFT is back channel etch (BCE) structure which is widely used for conventional a-Si TFT. It means no addition mask process is needed, so GaInZnO TFT could be realized without cost increase compared with conventional a-Si TFT. For gate line, Mo metal was deposited by sputtering process. SiN film was deposited by plasma enhanced CVD process for gate insulator. 70nm GaInZnO film was formed by RF sputtering process. In order to control the electrical characteristics of GaInZnO film, Ar and O_2 gas flow was controlled during deposition. For data line Mo film was deposited by sputtering and dry etched. SiO_2 film was deposited for passivation layer. Plasma power and gas flow rate was optimized during passivation layer deposition in order to control the conductivity of GaInZnO film. After fabricating GaInZnO TFT, it was annealed at 200^{o}C for defect curing.

3. Results and discussions

In order to control the electrical characteristics of

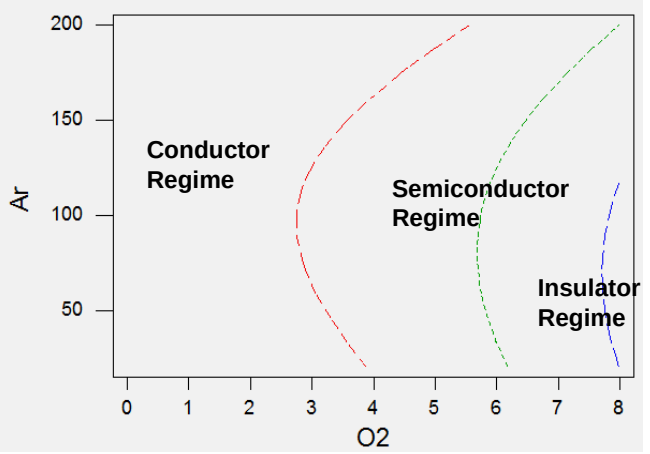

Fig. 2. Electrical property of GaInZnO TFT as a function of oxygen and argon flow rate during deposition

GaInZnO film, TFT of which channel was deposited by various deposition conditions (Ar flow rate and O_2 flow rate) was fabricated. When oxygen flow rate is low, GaInZnO film is not albe to adaptable for channel layer of transistor because the conductivity of film is high. When oxygen flow rate is high (over 8sccm), GaInZnO film was insulator. In the middle oxygen flow rate (5 ~8 sccm), GaInZnO shows semiconductor characteristics and suitable for channel layer. It is thought that as oxygen flow rate decrease the oxygen vacancies in deposited film and increase

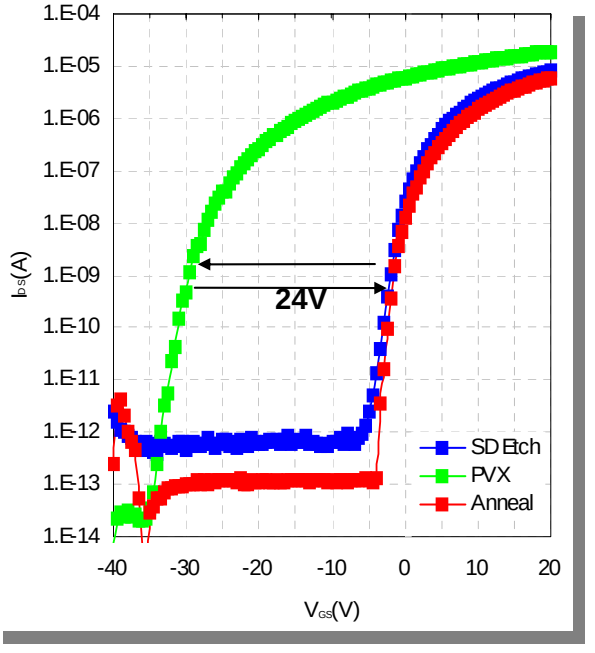

Fig. 3. The variation of TFT characteristic after passivation and post annealing process

electrical conductivity.[1,2] In the case of Ar gas flow, even though it is not strongly related to electrical property of GaInZnO film, it is one of the key parameter to control the uniformity of TFT behavior.

Figure 3 indicates the variation of transfer curve of GaInZnO TFT after passivation and post annealing process. The passivation SiO_2 film was deposited by PECVD at 150°C with SiH4 and N_2O gas. After passivation layer deposition, transfer curve of TFT was shift to negative by 24V and come back to original position after annealing at 200°C. In order to find out this reason, GaInZnO TFT was exposed to NH3 plasma before passivation (Fig. 4). After exposure, threshold voltage was move to -180V from 0V and come back to around 0V after annealing. Therefore, it is thought that hydrogen which comes from SiH4 gas during deposition of passivation layer generates oxygen vacancies in GaInZnO film and makes GaInZnO film conductive.[1]

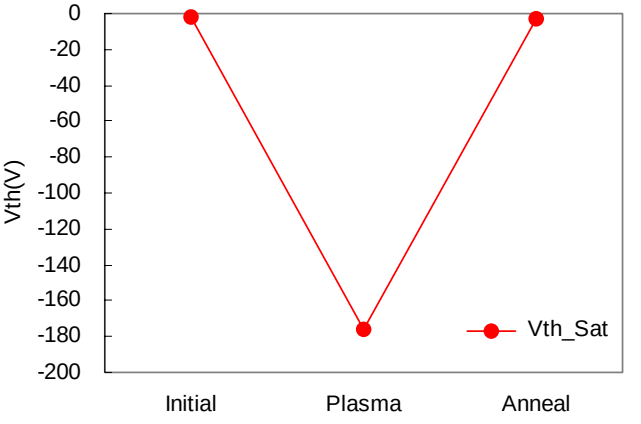

Fig. 4. Threshold voltage shift fo GaInZnO TFT after NH3 plasma treatment and post annealing process

Figure 5 shows transfer characteristics of optimized GaInZnO TFT compared with conventional a-Si TFT. The average mobility of GaInZnO TFT was measured at 2.6 cm^2/Vs which is 5 times higher than that of conventional a-Si TFT. Vt of GaInZnO TFT was measured at 3.8V. As mentioned, in the case of GaInZnO TFT, Vt was strongly dependent on process condition such as plasma condition for source- drain dry etch and deposition of passivation layer. By the controlling these process conditions, the standard deviation of Vt which is key indicator of TFT uniformity was reduced to 0.7V. Ion/Ioff was measured over 1E8 which is large enough to drive

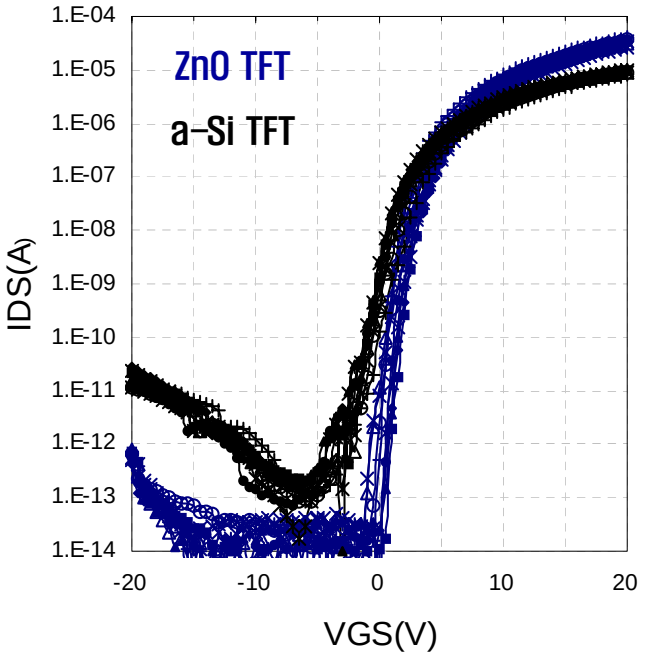

Fig. 5. Transfer characteristics of GaInZnO TFT

Table I. Summary of GaInZnO TFT characteristics

	Mobility	Vth	Ion/Ioff	S.S.
GIZO TFT	2.6±0.20 (cm2/Vs)	3.8±0.7 (V)	3.4E8	0.85±0.10 (V/dec)
a-Si TFT	0.6±0.03 (cm2/Vs)	1.1±0.6 (V)	9.3E7	0.94±0.04 (V/dec)

OLED or LCD. TFT characteristics were summarized at table I. Most process for fabrication of GaInZnO TFT array was carried out below 200°C including post annealing process except gate insulator deposition process (350°C).

After fabrication of TFT array, pixel electrode was deposited by DC sputtering process. And bank was formed by spin coating process. EL material was deposited by conventional evaporation technique. Finally 4 inch AMOLED was successfully drived by GaInZnO TFT array. AMOLED display image was shown in figure 6. The specification of AMOLED display was summarized in Table II.

Figure 7 indicates transfer characteristics of GaInZnO TFT fabricated at low temperature. The

Fig. 6. AMOLED display driven by GaInZnO TFT

Table II. AMOLED Display specification

Item	Specification
Size	4.0 inch (diagonal)
Resolution	320(H) x RGB x 240(V) [QVGA]
Pixel pitch	255 μm x 85 μm 100 ppi
Aspect ratio	4:3
Pixel design	2 Tr & 1C
OLED design	Bottom emission
Aperture ratio	25%

whole process for TFT fabrication was done below 150°C. After that, TFT was annealed at 200°C for 1 hour. Even though leakage current was increased by 1~2 orders compared with 350°C process, the mobility is large enough to drive OLED and LCD. Therefore, it is thought that high performance GaInZnO TFT could be realized on cheap substrate such as soda-lime glass or plastic for cost reduction.

4. Summary

4 inch QVGA AMOLED display with GaInZnO TFT was demonstrated. Because the structure of GaInZnO TFT is same with that of a-Si TFT, high performance TFT could be realized without cost increase. In addition, cheap substrate such as soda-lime glass or plastic could be adapted, because process was done

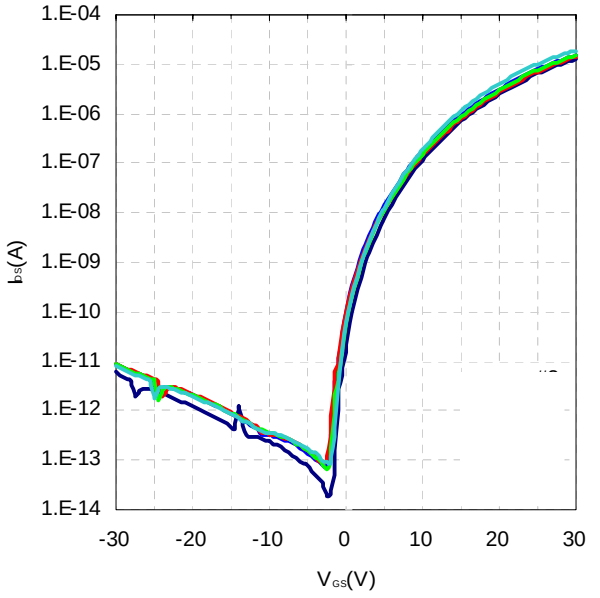

Fig. 7. Transfer characteristics of GaInZnO TFT fabricated below 200°C including post annealing process

below 200°C including post annealing process. It is considered that AMOLED TV and High resolution and speed AMLCD TV could be realized in near future by using electrical stable, uniform in large area, cheap process available GaInZnO TFT.

5. References

1. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, *Nature*, **432**, 488 (2004)
2. H. Yabuta, M. Sato, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, A*ppl. Phys. Lett.*, **89**, 112123 (2006)
3. K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano and H. Hosono, *Science*, **300**, 1269 (2003)
4. R. L. Hoffman, B. J. Norris and J. F. Wager, *Appl. Phys. Lett.*, **82**, 733 (2003)
5. Y. Kwon, Y. Li, Y. W. Heo, M. Jones, P. H. Holloway, D. P. Norton, Z. V. Park and S. Li, *Appl. Phys. Lett.*, **84** 2685 (2004)