Technical Obstacles to Suftla Flexible Microelectronics

Mitsutoshi Miyasaka

Advanced Product Development Department, Seiko Epson Corporation
281 Fujimi, Fujimi, Nagano, 399-0293 Japan
E-mail: miyasaka.mitsutoshi@exc.epson.co.jp
Keywords : TFT, Plastic, Self-heating, Durability, Yield

Abstract

Three technical obstacles must be overcome to build a fruitful business in the nascent industry of flexible microelectronics: the self-heating effect of thin film transistors (TFTs), the thermal and mechanical durability of flexible devices, and the cost issue. The self-heating effect is controlled through TFT shape, TFT electrical performance, dimensional reduction and energy-efficient circuits. Plastic engineering is one of the keys to solving thermal and mechanical durability problems faced by flexible microelectronics devices. For the Suftla flexible microelectronics business to be viable, Suftla transfer yield must be sufficiently high to keep down device cost. Improving the transfer yield is not easy, but it is the same challenge already faced and cleared in the TFT liquid crystal display industry.

1. Introduction

For more than half a century semiconductor devices have continued their remarkable advancement in terms of quality and market expansion. It has been this advancement that has enabled us to enjoy the high standard of living achieved in the last century. Because of the rewards that have been reaped in terms of quality of life, we hope for further advances in semiconductor technology. At the same time, however, the technology is widely believed to be on the verge of reaching its limits. The current scaling down of device geometries reminds us that materials are not infinitely divisible. In addition, the technical advantages of semiconductor devices with fine design rules may offset by higher fabrication costs. In the not-too-distant future the progression of semiconductor devices along the scaling rule will reach either its business or theoretical limit.

Another way of improving the semiconductor industry is to make the devices flexible. Flexible semiconductor devices have tremendous potential in the fabrication of future smart electronic devices, such as paper-like sheet displays [1, 2], artificial skin (flexible two-dimensional sensors) [3], and intelligent clothes. Hopes are high for thin, lightweight, flexible electronic devices. Therefore, many semiconductor researchers, especially those who study thin film transistors (TFTs), have been working to realize electronic devices on plastic (plastic device) [4 - 10]. Unfortunately, however, it is not widely recognized that there are still some important technical obstacles to achieving TFT devices and circuits formed on plastic.

This paper clarifies the main technical obstacles related to plastic devices and describes the basic strategies for overcoming them.

Table 1 Thermal conductivity

Solid	Thermal conductivity at 300K
Aluminum	239 $W\ m^{-1}\ K^{-1}$
Silicon	148 $W\ m^{-1}\ K^{-1}$
SiO_2 glass	1.38 $W\ m^{-1}\ K^{-1}$
Plastic films	~ 0.2 $W\ m^{-1}\ K^{-1}$

2. Self-Heating Effect

While transistors are in the on-state, the source-drain current generates Joule's heat, which raises the temperature of the transistors themselves [11]. This effect, known as self-heating, is one of the most important obstacles when dealing with plastic devices, because the thermal conductivity of plastic is very low compared with typical solids employed in TFTs (Table 1). The low thermal conductivity of plastic film prevents heat from dissipating from the semiconductor layer of a TFT and, consequently, the device temperature easily rises. In addition, in future plastic devices TFTs will be sandwiched between protective films to improve mechanical and environmental durability [12]. These protective films further prevent the dissipation of heat from the TFTs. Hence, given identical performance values, TFTs used in the flexible microelectronics industry exhibit greater susceptibility to self-heating than do TFTs used in the current glass-based liquid crystal display (LCD) industry.

Usually the glass transition temperature Tg of plastic film, which is roughly between 100°C and 200°C, determines the acceptable temperature levels of plastic devices. Above these temperature levels TFTs will certainly be damaged due to the thermal deformation of the plastic material. Controlling the self-heating effect is thus one of the most important obstacles faced by plastic device developers.

Self-heating can be controlled by four methods: the shape of the TFT, the TFT's electrical performance characteristics, dimensional reductions within the TFT, and the adoption of energy-effective circuits. Future plastic devices will need to be designed with some or all of these solutions in mind.

The efficiency of heat dissipation from the active semiconductor layer depends on the shape of the TFT. TFT shape thus has to be carefully designed to maximize dissipation efficiency [13]. The area in a transistor that reaches the highest temperature due to the self-heating effect is observed in the central area of the transistor, because heat generated in the semiconductor island radiates laterally from the island edges. Consequently, a TFT with a wide gate-electrode (large-W TFT) heats up more easily than a TFT with a narrow gate-electrode (small-W TFT) [11]. The efficiency with which heat dissipates from the large-W TFT is clearly too poor to enable the use of large-W TFTs in future plastic devices. When the functionality of a large-W TFT is required on plastic, parallel connections of plural small-W TFTs should be used.

Self-heating can also be limited by improving TFT electrical performance and by reducing TFT device dimensions. As a transistor originates from a transfer resistor, different states of electric resistance, or in other words different values of electric current, of transistor are utilized in all the integrated circuits.

Strictly speaking, the on-state current value of a transistor differs from application to application, though very roughly speaking an on-state current value of several hundreds of μA is widely used in many TFT applications. Since the power is a product of the drain current and the drain voltage, and since the on-state drain current is almost fixed to several hundreds μA, the drain voltage needs to be lowered to limit both power and self-heating. Five methods for obtaining the desired on-current value when the drain voltage is lowered have been identified:

(1) Short gate length (small L, dimensional reduction)
(2) Wide gate width (large W, unacceptable)
(3) Large oxide capacitance per unit area (thin gate-oxide layer, dimensional reduction)
(4) Large mobility value (high performance TFT)
(5) Low Vth value (high performance TFT)

The second of these five methods—a wide gate-electrode—is unacceptable due to poor heat dissipation efficiency. The fourth and fifth methods mean that TFTs used in plastic devices must exhibit high performance, possessing large mobility and small Vth values to drive the circuits on plastic with low drain voltage. The first and third methods involve a "scaling rule" that is similar to, but slightly differs in important ways from, the standard scaling rule employed in single-crystal silicon MOSFET devices. The newly proposed "TFT scaling rule" scales gate length L to L/k, gate-oxide thickness tox to tox/k, and voltage V to V/k, but keeps gate-width W and circuit area A the same. The drain current Ids therefore remains the same before and after TFT scaling, as does the gate-capacitance Cg. The power after TFT scaling is reduced to $1/k$ of the power before TFT scaling. Since we do not scale the circuit area A, the transistor density (number of transistors per unit area) does not change, and the power density (power generated per unit area) after TFT scaling is reduced to $1/k$ of the power density before TFT scaling. The TFT scaling rule effectively reduces both power and power density. In addition, circuit delay time τ is reduced to τ/k, and thus the operating frequency f speeds up to kf. The newly proposed TFT scaling rule will effectively limit self-heating as well as speed up the circuit operation.

Sophisticated circuits can also reduce the power while achieving the desired functionality. An example is the asynchronous circuit system [14, 15]. Nearly all conventional large-scale integration (LSI) devices are classified as synchronous circuit systems, in which a global clock signal is supplied to every circuit block. Even though some circuit blocks did not work and therefore did not need the clock signal, the global clock would always be supplied to all the circuit blocks. As a result, the clock-related circuits, such as clock buffers and opposite-phase clock generators, are always working and thus TFTs used in these circuits are susceptible to self-heating. In contrast to synchronous circuit systems, asynchronous circuit systems are clockless integrated circuits, in which each circuit block is activated only when needed. Normally, only a few circuit blocks in an LSI system must work simultaneously. In an asynchronous circuit system only those circuit blocks that need to work are working; the other circuit blocks are left idle. In other words there rarely are TFTs that work all the time and nearly all the TFTs have their own idle periods, even while the asynchronous circuit system is actively working. During this idle period the Joule's heat dissipates from each transistor. Asynchronous circuit systems, in fact, considerably reduce energy consumption, operate at cool temperature, and thus limit the self-heating effect of the component TFTs. Future plastic devices should incorporate asynchronous or other sophisticated circuit designs to limit the self-heating effect.

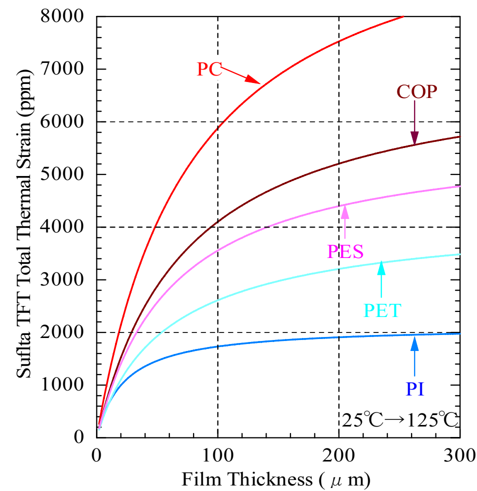

Fig. 1 Total thermal strain of of the 2-μm-thick TFT layer.

Abbreviations are as follows: PI = Polyimide, PET = Polyethyleneterephthalate, PES = Polyethersulfone, COP = Cycro-olefine polymer and PC = Polycarbonate.

Future smart plastic devices will need to be designed with some or all of these solutions in mind.

3. Device Durability and Plastic Engineering

The durability of plastic devices is another important technical obstacle to be overcome. Flexible microelectronics is defined as any form of TFT LSI circuit on plastic. Since TFT circuits are composed mainly of fragile glass (SiO_2) layers and since the plastic film is flexible, the circuits are very easily damaged. Plastic devices, which are susceptible to cracking, must be durable enough to withstand the fabrication process as well as practical use. Here, two kinds of durability should be considered, namely thermal and mechanical durability. In terms of thermal durability, cracks must not be formed during the fabrication process. Devices have to withstand a temperature difference of approximately 100°C. Durability in practical use is slightly easier. Mechanical durability during practical use is more severe, because devices ideally should withstand a very small curvature radius so that they can be folded.

Cracks form in plastic device because the strain on the TFT layer is larger than the elastic limit of the TFT layer. Therefore, to prevent the TFT layer from being cracked, the TFT strain must be kept lower than the elastic limit. Small TFT strain values improve device durability.

The thermal strain of the TFT layer $\Delta\varepsilon_T$ is expressed by

$$\Delta\varepsilon_T = \frac{(c_F - c_T)\Delta T}{\dfrac{Y_T d_T}{Y_F d_F} + 1} \quad (1),$$

where c_T and c_F are the coefficient of thermal expansion (CTE) of the TFT and the film, respectively, Y_T is the Young's modulus of the TFT, Y_F is that of the film, d_T is the TFT thickness, d_F is the film thickness, and ΔT is the temperature difference [16]. The integral of the equation (1) from room temperature T_R to high temperature T_H gives the total thermal strain ε_T

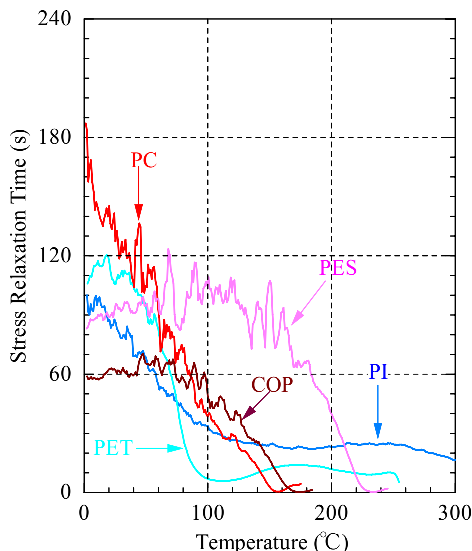

Fig. 2 Stress Relaxation Time of films

$$\varepsilon_T = \int_{T_R}^{T_H} \frac{(c_F - c_T)}{\frac{Y_T d_T}{Y_F d_F} + 1} \mathrm{d}T \qquad (2).$$

TFT circuits crack when the total thermal strain ε_T is larger than the elastic limit of the TFT circuit. The equation (2) indicates four methods to prevent the TFT circuit from being cracked during the thermal process: a small temperature difference, a small CTE difference, and small Y_F and d_F values. Figure 1 is the calculated total strain of the 2-µm-thick TFT layer, when the TFT layer is formed on various plastic films and is heated up from 25°C to 125°C, as a function of the film thickness, using the equation (2), and Y_F and c_F values that are actually measured. Polyimide film least stretches the TFT layer owing to it smallest c_F value. Since it is reported that the elastic limit of the TFT layer is approximately between 3000 ppm and 5000 ppm [17], any plastic films shown in Fig. 1 except for Polycarbonate can be used as the base film if the film thickness is less than 100 µm.

Discussions so far assume that the film is an elastic body. In fact, however, it is a viscoelastic body and possesses a viscous fluid nature especially at high temperature. The viscous flow of the plastic film can relax the thermal stress, so as to reduce the strain. The stress relaxation time (SRT) τ is expressed by

$$\tau = \frac{\eta_F}{Y_F} \qquad (3),$$

where η_F is the coefficient of viscosity of the film. If the SRT is significantly shorter than the temperature changing period (during which the film temperature changes between T_R and T_H), the thermal stress will be immediately relaxed and, therefore, the strain ε_T will always be very small. The shorter SRT can improve the durability of a plastic device. Since a small value for the Young's modulus of the film is preferable according to the equation (2), a small coefficient of viscosity value for the film is also preferable. Figure 2 is the measured SRT dependence on temperature. Cycro-olefine polymer possesses fairly short SRT value over the practical temperature ranges, though the value is, unfortunately, too large to relax the thermal strain during the practical fabrication process.

The mechanical strain of the TFT layer ε_M is expressed by

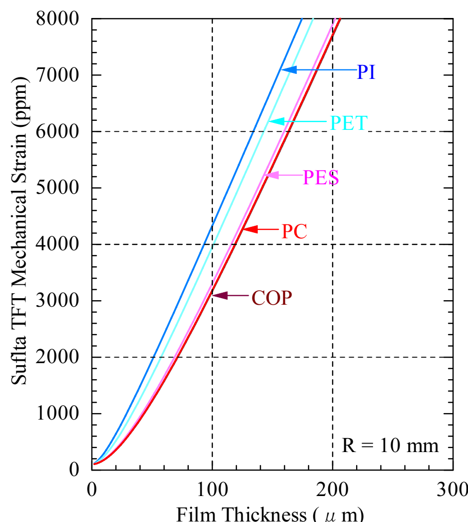

Fig. 3 Mechanical Tensile Stress of the 2-µm-thick TFT layer, when outward bended

$$\varepsilon_M = \frac{d_T + d_F}{2R} \cdot \left\{ \frac{1 + 2\cdot\frac{d_T}{d_F} + \frac{Y_T}{Y_F}\cdot\left(\frac{d_T}{d_F}\right)^2}{\left(1+\frac{d_T}{d_F}\right)\left(1+\frac{Y_T d_T}{Y_F d_F}\right)} \right\} \qquad (4),$$

where R is the curvature radius [18]. When the TFT layer is far thinner than plastic films, the equation (4) is simplified to

$$\varepsilon_M = \frac{d_T + d_F}{2R} \cdot \frac{1}{1 + \frac{Y_T d_T}{Y_F d_F}} \qquad (5).$$

It is noticed that small values of Young's modulus and film thickness are effective for reducing the mechanical strain. Figure 3 is the calculated mechanical tensile strain of the 2-µm-thick TFT layer, when the TFT layer is outward bending with the curvature radius of 10 mm, using the equation (4). Polyimide film stretches the TFT layer the most because it has the largest Y_F value. For improved thermal durability of the plastic device a plastic film should possess a small CTE value and a small Young's modulus. The Young's modulus of a film, however, generally increases in inverse proportion to the CTE value. Films that have a small CTE value and are thus suitable for improving the thermal durability tend to possess a large Y_F value, which adversely affect the mechanical durability.

The best film for plastic devices must be selected by simultaneously considering the CTE value as well as the Young's modulus and film thickness.

4. Cost and Yield

Suftla technology [8, 9] is seen as a prime enabler of a life-enhancing flexible microelectronics industry, but cost is a critical issue. It is essential that Suftla be cost-effective. The original TFT substrates used in the Suftla process are fabricated in a process that differs from a standard low-temperature polysilicon (LTPS) TFT process only in that an additional a-Si film is deposited as a sacrificial layer. The additional deposition step does not dramatically increase Suftla cost. The original TFT substrates thus cost approximately the same as standard LTPS TFT substrates.

In addition, the Suftla transfer process is rather simple and does not require very expensive manufacturing equipment, such as photolithography and chemical vapor deposition systems. As a result, the Suftla process can cost far less than an LTPS TFT process. The price of Suftla flexible devices must unavoidably be slightly higher than that of standard LTPS TFT substrates. However, this cost estimate assumes a Suftla transfer yield of 100%. Needless to say, if the transfer yield is 50%, the cost will double. The cost of Suftla devices is totally dependent on the transfer yield. Accordingly, another technical obstacle is to increase Suftla transfer yields.

The Suftla transfer yield depends on the size of the device. Large devices suffer from a poor yield; by contrast, small devices enjoy a high yield. The Suftla transfer yield is expressed with the exponential distribution

$$g(S) = \int_S^\infty f(s:\alpha)ds = e^{-\alpha S} \quad (6),$$

where α is the defect rate [16]. The Suftla transfer yield decreases exponentially as device area increases. A viable Suftla flexible microelectronics business with minimal Suftla cost would require a very low defect rate, probably a rate less than 2.5×10^{-5} cm^{-2}. This would mean a Suftla device transfer yield of more than 98%, liberating Suftla from the cost issue. Attention to costs involving Suftla devices would then shift to the standard LTPS TFT substrate.

As discussed above, Suftla transfer yield must be as high as possible. The sources of the transfer defects are thus systematically analyzed in an effort to raise yields. TFT LCD engineers would find the defect sources quite familiar. Air bubbles in the adhesive layer are one source. The bubbles prevent the TFT layer from adhering to the temporary substrate, thus inducing transfer defects. This example is similar to air bubbles in the liquid crystal layer in the TFT LCD industry. Other examples of the sources of defects are adhesive-repellent spots, dust and particles, adhesive degradation, and static electricity. The TFT LCD industry once faced these same problems. Reducing the defect rate in the Suftla process to less than 2.5×10^{-5} cm^{-2} will not be easy, but these problems will eventually be cleared, just as they were in the TFT LCD industry.

5. Conclusions

Plastic devices—TFT LSI circuits on plastic—will enable next-generation electronics that will enhance our lives in the near future. Before attractive plastic devices can be achieved, however, technical solutions must first be found for three problems: the TFT self-heating effect , flexible device durability, and cost.

Self-heating can be controlled through TFT shape, TFT electrical performance characteristics, dimensional reductions within TFTs, and the adoption of energy-effective circuits.

To improve thermal and mechanical durability of flexible devices, the TFT strain must be as low as possible. Plastic engineering is one of the keys to solving the durability problems. Plastic films must be engineered so that they are thin and possess small CTE, Young's modulus and viscosity values. Since films that possess a small CTE value tend to have a large value for Young's modulus, the best film for plastic devices must be selected by simultaneously considering the CTE value as well as the Young's modulus and film thickness.

Suftla technology is seen as a prime enabling technology, but Suftla transfer yields must be sufficiently high to keep down device cost. The transfer yield decreases exponentially as device size increases. Improving the transfer yield of large devices to nearly 100% will not be easy, but the same challenge has already been faced and cleared in the TFT LCD industry.

Once these obstacles are cleared, Suftla could be a driving force behind the nascent flexible microelectronics industry.

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