Thickness-dependent morphology of ZnO films and amorphous ZnO Transparent TFT

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Abstract

Thickness dependent morphology of ZnO films was studied, and ZnO can be intentionally grown into amorphous phase by reducing the thickness. The top-gate amorphous ZnO TTFTs with rather high field-effect mobilities and on/off current ratios were effectively fabricated.

1. Introduction

Oxide-semiconductor-based thin-film transistors (TFTs) have advanced tremendously recently, and have provided an attractive alternative to silicon-based TFTs or organic TFTs [1-3]. Oxide semiconductors composed of heavy-metal cations with $(n-1)d^{10}ns^{0}$ $(n \geq 4)$ electronic configurations have been widely investigated due to their several merits such as high mobilities, high transparencies, and low processing temperatures [4-7]. Compared to the polycrystalline oxide semiconductors, the amorphous oxide semiconductors are more preferred because of their lower processing temperatures, better uniformity and sometimes even higher field-effect mobility due to lacks of grain-boundary issues.

Since ZnO easily forms the polycrystalline phase even at room temperature, researchers usually mix several kinds of heavy-metal oxides in order to prevent crystallization. In this paper, thickness dependent morphology and crystallinity of ZnO films are studied. We show that by reducing the thickness of ZnO films, ZnO can be intentionally grown into the amorphous phase. Such simple and effective approach of directly forming amorphous ZnO can be used in device applications. We also report the top-gate amorphous ZnO TTFTs with rather high mobilities fabricated by all-etching processes.

2. Experimental

Fig. 1 shows the schematic structure of the top-gate ZnO transparent TFTs studied in this work. Patterned 120-nm ITO on glass substrates was used as the source and drain electrodes. The ZnO channel layer of various thicknesses was deposited by RF sputtering in Ar/O_2 without intentional heating of the substrates. 50-nm SiN_x was then deposited by plasma enhanced chemical vapor deposition (PECVD) at 200 ºC to serve as the ZnO etching mask and the passivation layer since ZnO can be easily damaged or degraded by chemicals used/produced during the lithographic processes. This SiN_x layer was first patterned by lithography and reactive ion etching (RIE) in CHF_3/O_2 and then was used as the hard mask for patterning ZnO. Next, the ZnO active layer was etched without damaging/etching the polycrystalline ITO. Subsequently, another 150-nm SiN_x was deposited by PECVD at 200 ºC to complete the gate insulator stack. The 120-nm ITO gate electrode was deposited by RF sputtering and was patterned by lithography and wet etching. Finally, the gate insulator was etched by RIE to expose the source/drain contact pads. The completed TTFTs together with the glass substrates show high transparency with the transmittance higher than 80% over the whole visible range (400~700 nm).

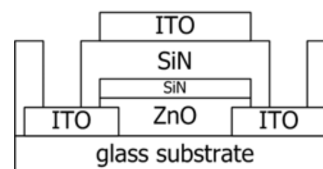

Fig. 1. Device structure of top-gate ZnO TTFT.

3. Results and discussion

ZnO thin films of various thicknesses were deposited on glass substrate by RF sputtering in Ar/O_2. A check of the topology and morphology of thin films by tapping mode atomic force microscope (TM-AFM) shows very different characteristics for thick and thin ZnO films. Figure 2(a) and 2(b) show the AFM phase images of the 10-nm and 60-nm ZnO films, respectively. While hardly any distinguishable grains are visible in the 10-nm ZnO film (indeed the AFM image is simply similar to that of a glass substrate), grains of tens of nm are clearly visible in the 60-nm ZnO film. The SEM images of the 10-nm and 60-nm ZnO films, shown in Figure 2(c) and 2(d) respectively, also show similar results.

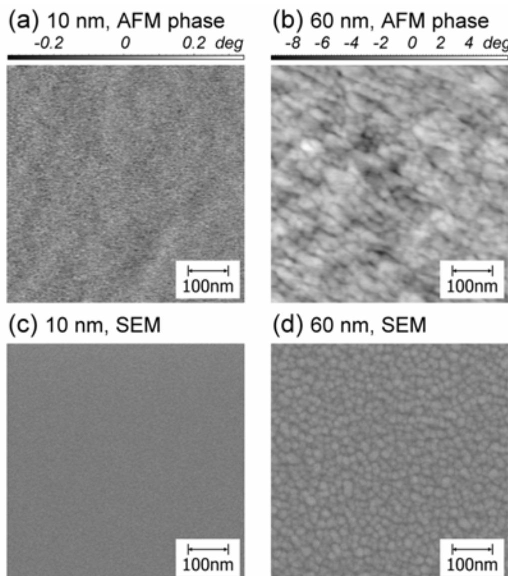

Fig. 2. AFM phase images of ZnO films with thickness of (a) 10 nm and (b) 60 nm, and SEM images of ZnO films with thickness of (c) 10 nm and (d) 60 nm.

The RMS roughnesses and the average grain sizes are derived from the AFM images for ZnO films of various thicknesses, as shown in Figure 3, further manifest such a difference. Both the RMS roughness and the average grain size show an evident increase for films thicker than 40 nm, but show a negligible change below 20 nm. All these results indicate the manifestation of phase transition from amorphous to polycrystalline structure with increasing ZnO film thickness. Studies on similar thickness dependent crystallinity of various materials have also been reported by researchers [8-10]. In the initial stage of the film growth, only very few and small nanocrystallitic islands may exist in the film (thus should be considered as amorphous film). As the thickness of the film increase, the islands coalesce and result in larger grain size and RMS roughness. Therefore, by decreasing the thickness of the ZnO film below some tens of nm, the smooth amorphous and grain-boundary-free ZnO films can be obtained.

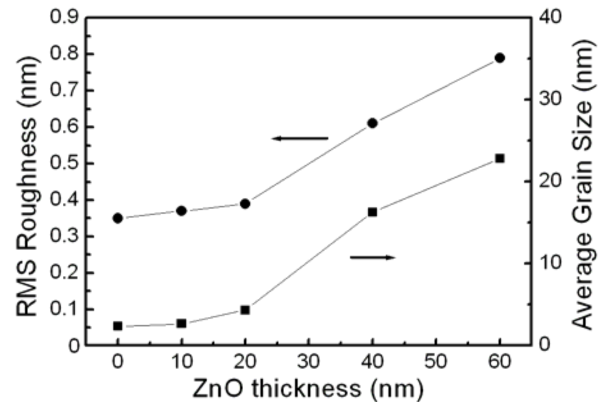

Fig. 3. The RMS surface roughness and the average grain size of the ZnO film as a function of the film thickness.

Using the 10 nm and 60 nm ZnO film as the active layer, we fabricated the top-gate ZnO transparent TFTs by using all etching processes. Although both devices were processed in similar conditions, the TTFT with 60-nm ZnO neither turns on nor shows transistor characteristics, yet the TTFTs with 10-nm ZnO show typical transistor characteristics in the n-type enhancement mode. Considering the polycrystalline characteristics of the 60-nm ZnO and the amorphous characteristics of the 10-nm ZnO, it is most possible that the present device processing conditions (with processing temperature only up to 200 ºC) is not sufficient to activate the polycrystalline ZnO (e.g. annealing the grain-boundary defects etc.) for TFT operation. In contrast, since there are no grain boundaries in the thin and amorphous ZnO, the as-fabricated TTFTs readily show well-behaved carrier transport and transistor operation. Figure 4 shows the representative output characteristics (I_D-V_{DS}) and the corresponding transfer characteristics (logI_D-V_{GS} and $\sqrt{I_D}$-V_{GS} in the saturation mode) of a top-gate TTFT with 10-nm ZnO active layer and W/L of 100/10 μm. From $\sqrt{I_D}$-V_{GS} in the saturation mode shown in Figure 4 (b), a high mobility of ~25 $cm^2/V\cdot s$ and a V_t of 4.53 V are extracted using the saturation

current equation of a field-effect transistor. Also from $\log I_D$-V_{GS} shown in Figure 4 (b), the subthreshold slope and the on/off current ratio are estimated to be 1.24 V/decade and $2.3x10^7$.

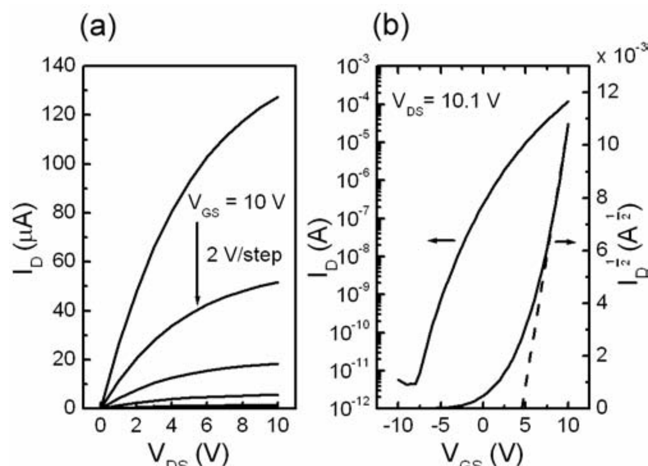

Fig. 4. (a) Output characteristics, and (b) transfer characteristics of a top-gate TTFT with 10-nm amorphous ZnO as active layer.

4. Summary

Oxide-semiconductor-based TFTs are becoming an important emerging technology in recent years due to their various merits and unique properties. In particular, amorphous oxide semiconductors and TFTs are aggressively pursued due to their lower processing temperatures, potentially higher mobilities and better uniformity suitable for high-performance displays and flexible electronics. Typically oxide semiconductors easily form in polycrystalline phase even at room temperature, and thus usually mixed oxides are used to grow amorphous oxide semiconductors. In this paper, we show that by simply reducing the thickness, oxide semiconductors can be intentionally grown into the amorphous phase, giving a simple and effective approach. Furthermore, we report the top-gate amorphous ZnO TTFTs with rather high mobilities fabricated by all-etching processes.

5. References

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