Advanced Amorphous Silicon TFT Backplane for AMOLED Display

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Abstract

We have investigated the degradation mechanism of hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) The threshold voltage of driving a-Si:H TFT is shifted severely by electrical bias due to a charge trapping and defect state creation. And the short channel TFTs exhibit less threshold voltage degradation than long channel TFTs. We propose the pixel circuits employing negative bias annealing scheme in order to suppression of threshold voltage shift of a-Si:H TFT.

1. Introduction

Active-matrix organic light emission diode (AM-OLED) displays have considered to an attractive display for flat-panel displays (FPDs) due to high brightness, fast response time, and wide viewing angle [1,2,3]. Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) have also a considerable attention for AMOLED backplane because of its good uniformity and established fabrication process [4,5]. However, the a-Si:H TFT is degraded severely by electrical bias during driving OLED, and the decrease of output current in a-Si:H TFT due to threshold voltage degradation causes a decrease of quality in AMOLED display [6].

The threshold voltage of a-Si:H TFT shifts in positive direction by the positive gate bias due to creating the defect state. Whereas the negative gate bias causes threshold voltage to shift in negative direction because of hole trapping [7]. Therefore pixel driving method applying the negative gate bias to a-Si:H TFT could suppress the threshold voltage shift of driving TFT of each AM-OLED pixel [8,9].

The purpose of this paper is to investigate the degradation mechanism of short channel a-Si:H TFTs, and the pixel driving methods, which can suppress the threshold voltage shift of a-Si:H TFTs.

2. The Degradation of Hydrogenated Amorphous Silicon

The a-Si:H TFTs exhibit a bias-induced metastability phenomenon that causes the threshold voltage shift in the presence of a gate bias [10]. The degradation mechanism of the a-Si:H TFTs under gate bias stress are the charge trapping in the gate insulator and the deep-state defect creation in the a-Si:H layer or at the a-Si:H / a-SiNx:H interface [11]–[14].

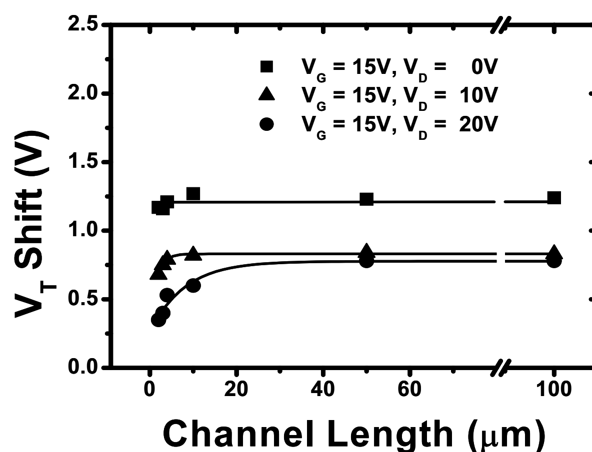

Fig. 1. Threshold voltage shift versus channel length for different applied voltages (W = 200 ㎛). The stress time is 30,000sec

Deep-state defect creation can be explained by the defect pool model [15], where the rate of defect creation is proportional to the number of carriers in the conduction band tail states. It also has been reported that if some bias is applied to the drain terminal, the induced carriers near to the drain decreases and this leads to the reduction of defect creation. As a consequence, smaller threshold voltage shift occurs if the drain bias exists [4].

Fig 1 shows the threshold voltage shifts after 30,000sec DC bias stress. When the TFT have been

suffered by the only gate bias stress (VG=15V, VD=0V), threshold voltage shift would not vary significantly with channel length, but in the presence of drain bias (VG=15V, VD=10V), threshold voltage shift decreased as the channel length reduced. Threshold votlage shift decreased more significantly in the higher drain bias stress condition (VG=15V, VD=20V).

Smaller threshold voltage shift in the short channel TFTs can be explained by the concentration of the channel charge varying with the drain bias. As the drain bias increases, the carrier concentration near the drain decreases [4]. Since the portion of the depleted charges over total charges induced in the channel increases with reducing channel length, the short channel TFTs has the smaller carrier concentration than the long channel TFTs. Because the defect state would be relative to the charge induced in the channel, short channel TFTs exhibit less threshold voltage degradation than long channel TFTs.

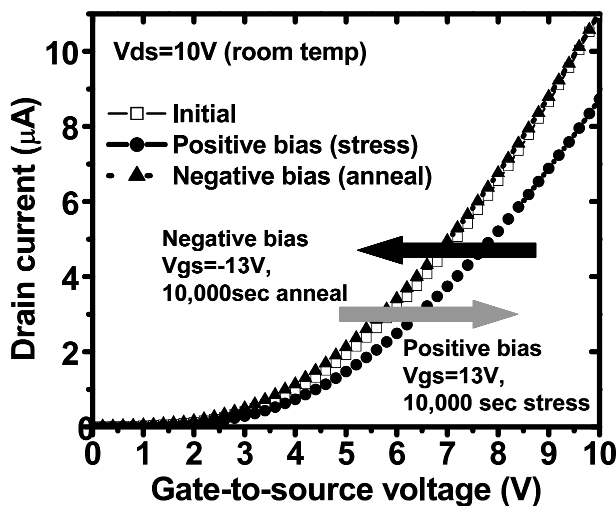

Fig. 2. Drain current curve to gate-source voltage of a-Si:H TFT (a) after positive bias stress and (b) after negative bias annealing

The positive bias stress causes an increase in the density of trap state, but negative bias stress with gate voltage mainly reduces the density of states. As shown in Fig. 2, the threshold voltage of a-Si:H TFT shift by gate bias stress. After a TFT is stressed by positive bias of 13V during 10000sec, the threshold voltage is shifted on the positive direction However, this TFT is again stressed by negative bias of -13V during 10000sec, threshold voltage is almost recovered to initial curve. Therefore the pixel circuit based a-Si:H TFT backplane should employ the negative bias annealing method which could restrain the degradation of a-Si:H TFT. Some driving schemes using a negative bias to reduce degradation of a-Si:H TFT itself are recently reported [8,9,16].

3. The pixel scheme for suppression of threshold voltage shift of a-Si:H TFT

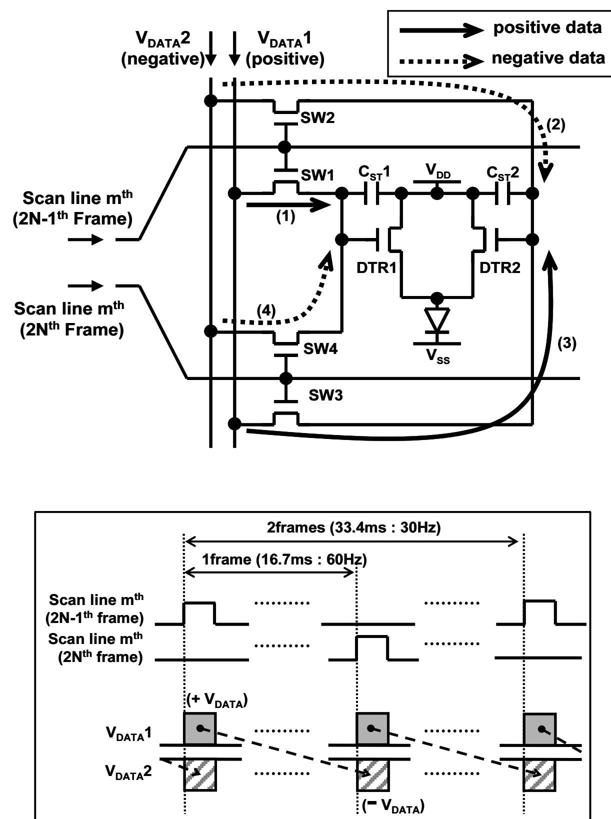

Fig. 3. The Polarity Balanced Driving (PBD) pixel circuit employing a negative bias annealing method and a timing diagram

Fig. 3 shows the pixel circuit and timing diagram of the polarity balanced driving (PBD) [8]. The pixel circuit mainly consists of two driving transistors (DTR1, DTR2) with storage capacitors ($C_{ST}1$, $C_{ST}2$) and switching transistors (SW1, SW2) to provide positive data. The switching transistors (SW3, SW4) to recover transistor characteristics with negative bias are also employed with dual scan and

data lines. The scan signal for selecting horizontal line is supplied through scan line every other frame.

When the scan signal is high, SW1 and SW2 (or SW3, SW4 in next frame) turn on. The data signal is stored at the connected capacitor with drain and gate of DTR1 (or DTR2) through switching transistor SW1 (or SW3). For example, the scan m ($2n-1^{th}$) is high in odd frame and this scan signal turns SW1 and SW2 on. According to the switching process, the storage capacitor ($C_{ST}1$) was charged by positive data ($+V_{data}$) to maintain data during one frame. The DTR1 allows to flow driving current to the OLED while DTR2 annealed by negative bias through $V_{data}2$ line.

SW3 and SW4 may operate in the same way in the even frame. The new method may be summarized as follows: each driving TFT (DTR1, DTR2), which has positively shifted threshold voltage during alternative frame, is annealed by negative bias when neighboring TFT operates.

The negative bias annealing by the PBD method could suppress the threshold voltage shift of driving TFT. However, the PBD scheme would need a double composition as conventional 2TFT pixel circuit, and reduce the aperture ratio of each pixel.

Fig.4 shows that the a-Si:H TFT pixel circuit employing fraction time annealing (FTA) scheme [9]. The negative bias comes from a clock signal line during a fraction of each frame in order to reduce threshold voltage shift of T2.

When a clock signal is larger than a data voltage, T3 is turned off because V_{GS_T3} is 0V. T2 can supply I_{OLED} according to the input data voltage so that threshold voltage of T2 increases due to a positive gate and drain bias stress. When a clock signal is low, T3 is turned on so that a gate node voltage of T2 would be discharged to the low state of clock signal. The negative bias of the clock signal is applied to the gate node of T2 so that the holes are trapped in SiNx insulator, so that an increased threshold voltage of a-Si:H TFT due to the positive gate and drain bias is reduced considerably. Although I_{OLED} stability in the negative bias annealed pixel is improved compared with conventional one, a gradual decrease of I_{OLED} in the negative bias annealed one may be attributed to the small β of a negative gate bias stress compared with β of a positive gate bias stress ($\Delta V_{TH} = A \cdot t^{\beta}$).

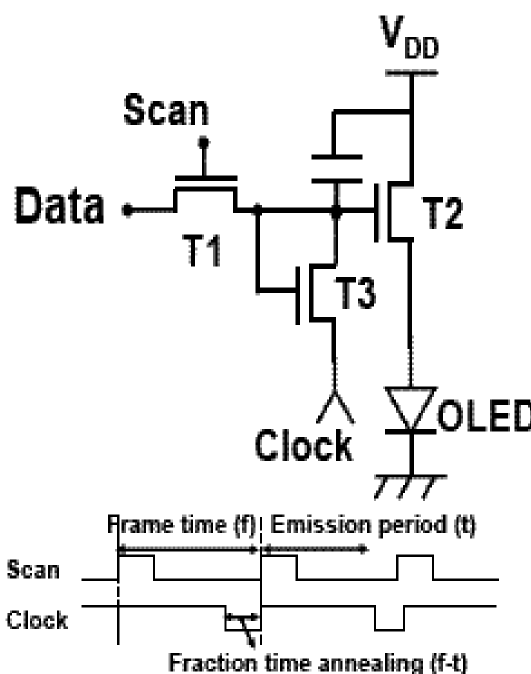

Fig. 4. The fraction time anneling (FTA) pixel circuit employing a negative bias annealing method and a timing diagram

However, the constant negative bias for recovering the degradation of TFTs was not fully signal-oriented in each pixel, and a proper compensation scheme should be followed for good screen uniformity.

As shown in Fig.5, polarity inversion driving (PID) scheme performs the negative bias annealing on a-Si:H TFTs during a fraction of one frame time [16]. The curing voltage is varied according to the degree of degradation of a driver TFT on which previous emitting gate bias was applied. It can suppress the threshold voltage shift and provide the good screen uniformity without any threshold voltage compensation scheme.

PID is basically a temporal interlacing method, which divides one frame into two periods, the operating period and the retrieving period. An original positive analog voltage is applied in the former period while the negative voltage based on the original image data in the latter one. As shown in Fig.5, the frame rate in the PID should be doubled and the positive pixel voltage, VDATAP and the negative voltage, VDATAN alternate according to the polarity selection signal, POL.

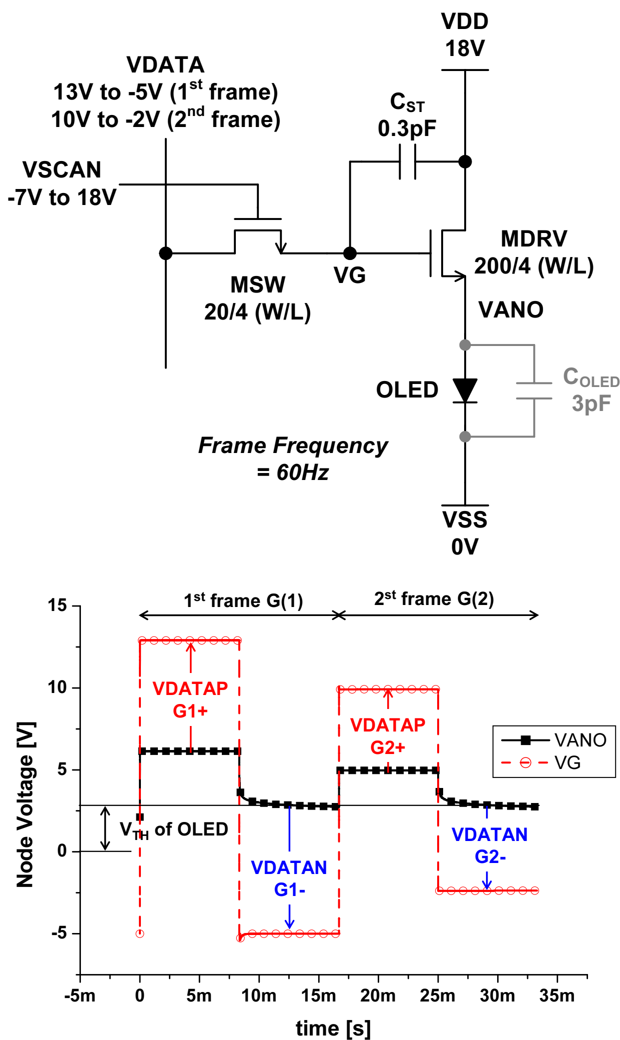

Fig. 5. 2-TFT pixel circuit employing the polarity inversion driving (PID) method, and Waveforms of VG and VANO

4. Conclusion

The a-Si:H TFT would have been a candidate for AMOLED backplane because of its good uniformity and established fabrication process. However, the degradation phenomenon of a-Si:H TFT is serious problem on the short channel TFTs rather than long channel TFTs. It is necessary for the pixel circuit to employ the negative bias annealing scheme for suppressing threshold voltage shift, such as the polarity balanced driving (PBD) method, the fraction time annealing (FTA) method, and the polarity inversion driving (PID) method.

5. References

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