

Analysis of the Horizontal Block Mura Defect

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Abstract

In TFT-LCD, mura is a defect which degrades the display quality. The resistance difference between gate lines is the main cause of H-Block mura. Two methods could eliminate this defect. A thinner gate layer or gate fan-out pattern decrease mura level. H-Block mura has been reduced after implementing the new schemes.

observe at L63 gray level shown in Fig.1. Bright lines occur in between the pads and dark stripes exist near the fan-out area. H-Block mura occurs in the fixed area with the different levels. Horizontal block mura doesn't hamper the use of display device, but it deteriorates image quality.

The H-Block mura is analyzed leading to a new fan-out area gate line design to remove this mura.

1. Objectives and Background

In the early years, CRT (Cathode Ray Tube) is the dominant display monitor. As the semiconductor manufacturing process evolves, a great deal of display technologies emerge and TFT-LCD (Thin Film Transistor Liquid Crystal Display) becomes the most promising and dominant display technology. It has the advantages of portable, energy saving, radiation less, planar and right-angle display, etc. It has been the trend of display industry to replace CRT with LCD^[1].

The Mura is display defect showing display gray level non-uniformity on the screen. Mura is detected by changing the display pattern to black pattern or other low gray level in the darkroom. Observing the screen from different angles, various types of mura could be seen on the screen^[4].

H-Block (Horizontal Block) mura on the screen demonstrates horizontal strip pattern, which is easy to



Fig. 1 Horizontal Block Mura

2. Experimental and Results

Gate line length is different in the gate pad area as shown in Fig. 2. On the panels with the H-Block mura, linear gate line pattern is used at the fan-out area.

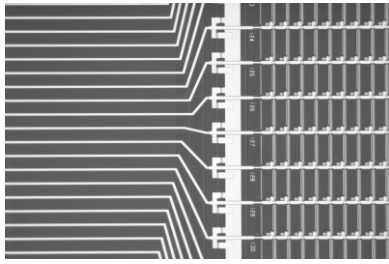


Fig. 2 Gate PAD Area Design

The fan-out area design aims to minimize RC delay and eliminate H-Block mura. The two test methods are listed below.

Two novel designs of zigzag pattern design and layer structure design are employed independently to eliminate the H-Block mura.

A. Zigzag Pattern Effect

On the panels with the H-Block mura, straight line type gate pattern is used at the fan-out area, resulting in the gate line length difference. In the pad center area, gate line is shorter and RC delay is smaller. In the pad edge area, gate line is longer and RC delay is larger. Shorter recharging time caused by RC delay results in smaller ΔV_p difference among the mura area and the normal area is the main cause of H-Block mura. The RC delay for each gate line is different. The gray display at the fan-out area is non-uniform^[3].

A zigzag pattern is used at the fan-out area to remove the RC delay non-uniformity.

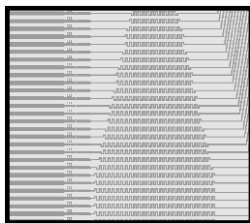


Fig. 3a Split 1

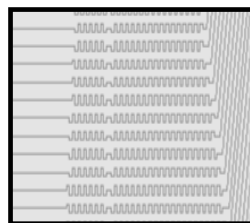


Fig. 3b Split 2

Fig. 3. Two Zigzag Patterns

Two zigzag patterns are shown in Fig. 3. Fig. 3a is the zigzag pattern with the tapered shape in the center area; Fig. 3b is the zigzag pattern near the pixel area.

These two designs aim to replace the line pattern with the winding pattern. They make the gate line length equally in the whole fan-out area^[5]. The shorter winding is employed at the longer gate line pattern area. The longer winding is used at the shorter gate line pattern area. The gate line resistance becomes uniform at the fan-out area eliminating H-block mura.

Table 1 lists the line resistance of the two designs. As shown in Table 1, split 2 has the minimal fan-out area resistance difference. The resistance difference between long and short line in split 2 is 178.1 Ω , which is lower than split 1 (182.6 Ω). Split 2 is the better one comparatively.

Table 1 Comparison of the two Zigzag designs

	Fan-out resistance, Ω	Δ (Long – Short), Ω
Normal	252.0 / 38.6	214.4
Zigzag (Split 1)	309.0 / 126.5	182.6
Zigzag (Split 2)	309.4 / 131.3	178.1

B. Layer Structure Change

An alternative method to eliminate H-Block mura is to reduce the gate line resistance. The RC delay non-uniformity could be decreased consequently.

Metal resistance is determined by the resistivity, cross sectional area and the length of the metal lines. To save the cost of adopting new metal, the gate metal thickness is changed to minimize the RC delay.

The resistance drops down when the layer becomes thicker and vice versa. The metal thickness is increased to reduce the square resistance of gate line and the RC delay^[6].

Table 2 Comparison between different Gate Thickness and Zigzag pattern

	Gate Thickness	Fan-out resistance, Ω	Δ (Long – Short), Ω
Normal	3000Å	252.0 / 38.6	214.4
	3600Å	207.6 / 31.8	175.8
Zigzag (Split 1)	3000Å	309.0 / 126.5	182.6
	3600Å	254.8 / 104.2	150.6
Zigzag (Split 2)	3000Å	309.4 / 131.3	178.1
	3600Å	254.8 / 108.2	146.6

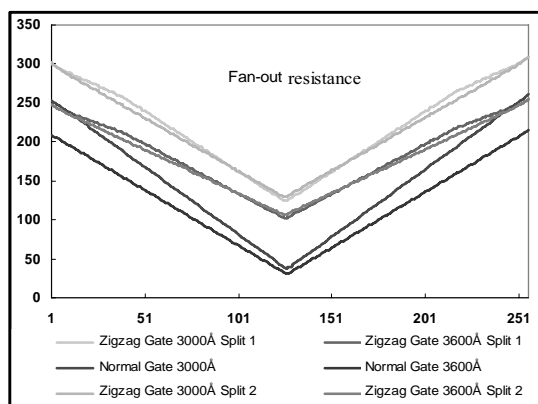


Fig. 4 Comparison between different gate line resistances

The results are compared in Table 2 and Fig. 4. Three different design were chosen: 1、normal design; 2、zigzag split 1 design; 3、zigzag split 2 design . Each split was divided into two different gate thicknesses. From table 2, it is found that fan-out resistance on all panels becomes smaller with increased gate thickness.

In Fig. 4, the horizontal axis is the gate line address in the fan-out region; the vertical axis is the line resistance. When gate metal thickness increases by 600Å, the resistance between different gate lines becomes identical. The combination of increasing gate thickness 600Å and the zigzag split 2, leads to the minimum gate line resistance difference.

3. Conclusion

The main cause of H-Block mura is the difference of the gate line resistance. Gate line length uniformity and gate line resistance reduction are proven to be critical eliminating the H-Block mura.

The test results show the H-Block mura has been reduced greatly after implementing the new gate line schemes.

4. References

- [1] Toshihisa Tsukada, TFT/LCD [M], Hitachi Ltd. Tokyo, Japan, 1996.
- [2] Lillis J, Cheng C K, Lin T T Y. Optimal wire sizing and buffer insertion for low power and a generalized delay model. IEEE J Solid-State Circuits, 1996, 31(3):437
- [3] Thomas L. Floyd, Principles of Electric Circuits Conventional Current Version Seventh Edition [M], Publishing House of Electronics Industry, 2005.
- [4] Harry J. Levinson, Principles of Lithography [M], the International Society for Optical Engineering. SPIE .2001 P97-104.
- [5] Sung Mo Kang, Yusuf Iblebici COMS Digital Integrated Circuits: Analysis and Design (Third Edition) [M], Publishing House of Electronics Industry, 2005.
- [6] L. Benini, G. De Micheli, E. Macii, "Designing low-power circuits: practical recipes," IEEE Circuits and Systems Magazine, Vol. 1, No. 1, 6-25 (2001).