# Study on the Stability of Organic Thin-Film Transistors Fabricated by Inserting a Polymeric Film as an Adhesion Layer

**Gun Woo Hyung[1,3], Il Houng Park [2,3], Ji Hoon Seo [2,3], Ji Hyun Seo [2,3], Hak Bum Choi[2,3] and Young Kwan Kim[2,3]***

[1] Dept. of Materials Science and Engineering, Hongik University, Seoul, Korea

[2] Dept. of Information Display, Hongik University, Seoul, Korea

[3]Center for Organic Materials and Information Devices, Hongik University, Seoul, Korea

*Phone: +82-2-320-1646, E-mail: kimyk@wow.hongik.ac.kr*

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## Abstract

*We demonstrated that the threshold voltage shift owing to a gate-bias stress is originated from the trapped charges at the interface between semiconductor layer and dielectric layer, and such drawback can be settled by applying long-term delay time to the gate electrode.*

## 1. Introduction

Organic electronics have shown remarkable progress on the necessary prerequisites such as organic thin-film transistor's device fabrication and materials optimization[1,2]. Negative gate bias stress causes a negative threshold shift, which was assigned to the trapping of charges in less mobile states located in the semiconductor, at the interface to the insulator or in the insulator itself. and the positive shift of the threshold voltage which occurs with a repetitive gate voltage sweep is due to the negatively charged traps inside the gate dielectric, which are injected from the gate electrode, without consideration of the polarization effect[3]. threshold voltage is an important parameter that needs to be controlled to ensure proper operation of the circuits. Here, we demonstrated that threshold voltage additionally depends strongly on the time period in which a gate voltage has been applied to bias stress. The capacitance-voltage (CV) characteristics of metal-insulator-semiconductor (MIS) structures adopting polymeric film formed by VDP method were also investigated.

## 2. Experimental

OTFTs had the ITO gate electrode and the $SiN_X$ gate dielectric. a polyimide film was codeposited by the high-vacuum thermal evaporation 6FDA and ODA at a pressure of $5\times10^{-7}$ Torr and a deposition rate of 5 Å/s, and cured at 150℃ for 1 h followed by 200℃ for 1 h in a vacuum oven at $5\times10^{-3}$ Torr. To adjust the balance of monomer's deposition rate to one to one, monomers were preheated for 2 hour before co-evaporation in the thermal vacuum chamber. The Ti used as adhesion metal layers between gold used as source/drain electrodes and gate insulator was deposited to through shadow mask inside thermal vacuum evaporator. Pentacene, which is *p*-type semiconductor layer with the thickness of 60 nm, was evaporated onto the polymeric adhesion layer and onto source and drain electrodes at room temperature by thermal vacuum evaporator.

Gate bias stress measurements were performed at room temperature for OTFTs with bottom-contact structures. The fabrication process and the electrical performance of bottom-contact structure are explained to the Appendix in detail. Transfer curves were taken from $V_G$ = +20 to -40 V (forward bias) and $V_G$ = -40 to +20 V (reverse bias) at 0.25 V steps during five times iteration in the same way on both configurations. Between transfer curves, the device was stressed for a time interval (t) at a fixed $I_D$ = 20V.

## 3. Results and discussion

The following profiles show the capacitance-voltage (CV) curves at room temperature for forward and reverse gate voltage sweep in metal-insulator-semiconductor (MIS) capacitors of Figure 1 (a) shows the CV curves for the gate voltage sweep from 20 V to -20 V and from -20 V to 20 V in MIS capacitors of ITO / 200-nm-thick $SiN_X$ as dielectric / 15-nm-thick 6FDA-ODA polymeric film as adhesion layer / 60-nm-thick pentacene at 10 kHz. As shown in MIS device using $SiN_X$ as insulators, the CV curves show a negative shift in the flat band voltage ($V_{FB}$) for the negative bias and a typical hysteresis effect that threshold voltage has been shifted in many OTFTs[4]. The CV curves show the accumulation at high negative voltages, and reduction of the absolute value of negative voltage decreases the capacitance down to a constant minimal value indicating that the layer is fully depleted. In case of organic semiconductors, the inversion region cannot be measured due to the long generation time of the wide bandgap material in high frequencies. Howev er, it is proposed that inversion should occur in organic transistors if the channel length is sufficiently small and if ohmic contacts for the minority carriers between the channel and both S/D electrodes can be prepared[5-7].

In the OTFT, the hysteresis behavior can be caused by mobile ions, change of dipoles or charge trapping in the gate dielectric. However, if the mobile charges were the cause of the hysteresis effect, the flat band voltage has to shift in the positive direction as positively charged mobile ions drift towards the gate during negative biasing. Also, if the change of dipoles in the gate dielectric was the cause of the hysteresis effect, the hysteresis difference of Figure 1 would show larger shift value. Usually, during charge trapping in the gate dielectric, electrons and holes from the gate or the pentacene semiconductor are injected into the gate dielectric, which is subsequently trapped. For a negative bias on the gate electrode, holes from the pentacene semiconductor can be injected into the gate dielectric, giving rise to a negative flat band voltage shift and electron from the gate electrode can be injected into the gate dielectric, giving rise to a positive flat band voltage shift. On the other hand, electrons from pentacene can be injected into the gate dielectric resulting in positive flat band voltage shift for a positive bias. However, flat-band voltage shifts to more negative during the return sweep of negative gate voltage. These results show that holes are injected into the gate dielectric from the pentacene semiconductor and electrons are not injected into the gate dielectric from the pentacene semiconductor. In case of OTFT using 6FDA-ODA polymeric film as gate insulator, hysteresis behavior and an accumulation region were not observed as shown in Figure 1 (b) because the current leakage flows into polymeric film. OTFTs using 6FDA-ODA polymeric film as an adhesion layer can reduce the hysteresis effect because of holes prohibited from being injected into the gate dielectric from the pentacene.

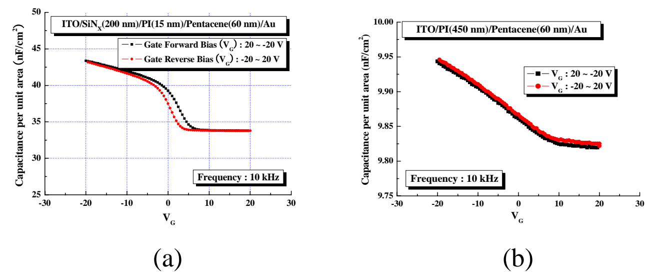


**Figure 1.** Measured CV curves of MOS capacitor with $SiN_X$ as gate insulator (a) and (b) a 6FDA-ODA polymeric film used as gate insulator at 10 kHz frequency.

Gate bias stress measurements were performed at room temperature for OTFTs with two different device structures (top-contact and bottom-contact structures). The fabrication process and the electrical performance of bottom-contact structure are explained to the Appendix in detail. Transfer curves were taken from $V_G$ = -40 to +20 V (forward bias) and $V_G$ = -40 to +20 V (reverse bias) at 0.25 V steps during five times iteration in the same way on both configurations. Between transfer curves, the device was stressed for a time interval (t) at a fixed $I_D$ = 20 V.

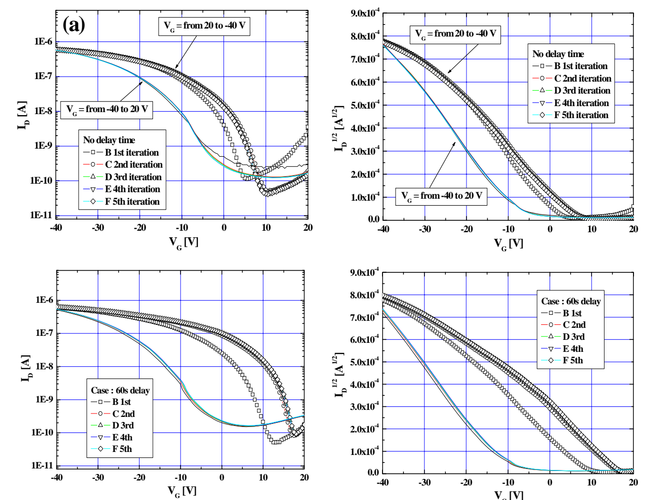


**Figure 2.** Logarithmic scale of forward and reverse transfer characteristics of OTFTs with 60 second delay time.

Figure 2 show a series of transfer curves at no delay time and 60 second in bottom-contact structures. Total stress time of 60 second causes a shift at threshold voltage of about 10 V during forward bias in the same way on both modes. Field-effective mobility and on/off current ratio are only negligibly affected by the bias stress.

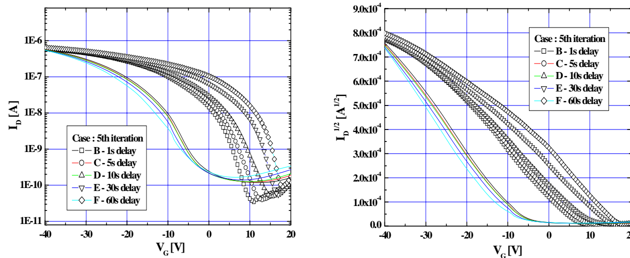


**Figure 3.** Transfer characteristics of OTFTs during fifth bias stress iteration; logarithmic (a) and linear (b) scales.

Figure 3 gives a summary of positive and negative bias stress measurements at different delay time. Between bias stress runs, the device was allowed to sit in light for 1 second to identical delay time with transfer curve of the 1 second delay time. For positive bias stress the threshold shift and the flat-band voltage are positive, whereas for negative bias stress the shift is towards more negative threshold voltage in both structures. The device eventually returns to its prestressed threshold voltage, however, the recovery can take days[8]. It was observed that light exposure decreased the recovery time, and so light exposure was used to reset the device between stresses. Similar bias stress effects were observed in both modes with 6FDA-ODA polymeric film and $SiN_X$ as gate dielectrics, implying that the specific chemistry of the interface between semiconductor and insulator is not the cause of the threshold voltage and the flat-band voltage shift.

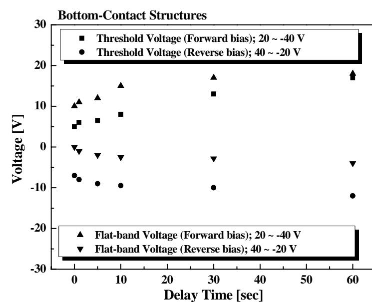


**Figure 4.** A change of threshold and flat-band voltages of forward and reverse biased OTFTs with different delay time in the bottom-contact structures.

Figure 4 shows a change of threshold and turn-on voltages of forward and reverse biased OTFTs with different delay time in the top-contact and in the bottom-contact structures. Bias stress effects involve charge-carrier trapping on a time scale faster than the total sweep time. As the forward sweep progresses, carriers are captured in trapping sites simultaneously screening the gate electric field, reducing the overall free-carrier concentration, and creating scattering centers. These results in a shift of flat-band voltage to larger gate voltage as the sweep progresses which, in turn, gives rise to a reduced $I_D$ upon reversing the gate voltage sweep because the difference of threshold voltage is smaller in the reverse bias. When forward negative gate voltage are used, both on and off current states of the OTFT could apparently shift toward more negative gate voltage[9,10]. It is clear that a shift can be observed between transfer characteristics measured by using forward and reverse sweeps. The observed hysteresis could be associated with the present mobile charge between the organic adhesion layer and organic semiconductor layer.

## 4. Summary

Consequently, it was confirmed that the threshold voltage shift owing to a gate-bias stress is originated from the trapped charges at the interface between semiconductor layer and dielectric layer, and such drawback can be settled by applying long-term delay time to the gate electrode. However, it was observed that the bias stress has little effect on the field effect mobility.

## 5. Acknowledgements

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