Dynamic Stress Analysis of a Bottom Gate TFT Having an Active Layer of Amorphous/Microcrystalline Si Double-Layers

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Abstract

We have fabricated bottom gate TFTs with active layers of amorphous/microcrystalline Si double layers (DL). Dynamic electric stresses were applied to DL TFTs and a-Si TFTs to compare their degradation characteristics. The DL TFTs were more stable under dynamic stresses than a-Si TFTs.

1. Introduction

The active matrix organic light emitting diode (AMOLED) has been widely studied. AMOLED displays have a wide viewing angle, a large color gamut, and a fast response time [1]. Because these displays are current driven, the backplane TFT should have highly uniform electrical characteristics. Amorphous Si (a-Si) TFTs have been intensively studied for AMOLED applications because the ease and high throughput of the deposition process make them easy to mass produce [1, 2]. However, a-Si TFTs have problems with low mobility and instability in AMOLED applications [3, 4]. Polycrystalline Si (poly-Si) based TFTs offer a high-field effective mobility, but show non-uniformity and their production process is problematic [5]. This paper explores the use of microcrystalline Si (μc-Si) TFTs to avoid these drawbacks [6]. Although μc-Si has a low deposition rate, μc-Si TFTs have a high-field effective mobility and show good stability under DC bias stresses [7].

We investigate the reliability of amorphous/microcrystalline Si double layers (DL) in the bottom gate TFT. We specifically focus on the degradation characteristics of both DL TFTs and a-Si TFTs under dynamic electric stresses.

2. Experiment

We propose a bottom gate TFT with an a-Si/μc-Si DL as an active layer. Figure 1 shows the schematic cross section of a typical DL TFT. The μc-Si layer was deposited in a 13.56 MHz capacitively coupled RF plasma enhanced chemical vapor deposition (PECVD) chamber. First, a 4000Å-thick Mo layer was deposited by sputtering, then the bottom gate was patterned. Four layers consisting of SiN_x (4000Å), a-Si (1000Å), μc-Si (1000Å), and n+ a-Si (1000Å) were then deposited by PECVD. The a-Si/μc-Si DL was created using mixtures of SiH_4/H_2/inert gas to form the a-Si layer, and SiF_4/H_2 to form the μc-Si layer. After defining the active channel region, a 4000Å-thick Mo layer was deposited by sputtering, then the source/drain electrode was patterned. Finally, a 2000Å-thick passivation layer of SiN_x was deposited.

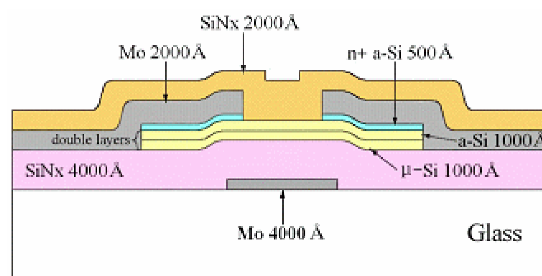


Fig. 1. Schematic cross section of the DL TFT

The fabrication process of DL TFTs is identical to that of conventional a-Si TFTs, and can be directly applied to the TFT fabrication process for commercial active matrix liquid crystal (AMLCD) without additional process steps or equipment. DL TFTs could be a cost effective way to mass produce AMOLEDs.

Figure 2 shows the plane image of the DL TFT (W/L = 50μm/8μm) and its channel area under an optical microscope.

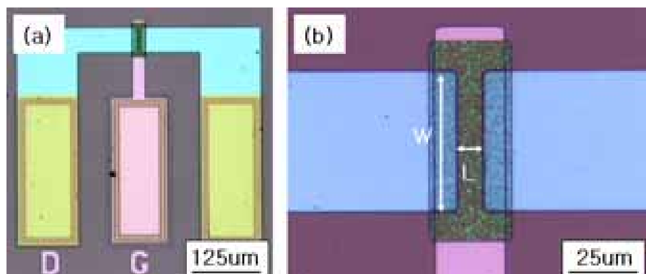


Fig. 2. The plane image of (a) the DL TFT (W/L = 50μm/8μm) and (b) the channel layer under an optical microscope

3. Results and discussion

Typical I_{ds}-V_{gs} transfer characteristics of the DL TFT with W/L = 50μm/8μm, are shown in Figure 3. The DL TFT has a field effect mobility of 0.44 cm^2/Vs, and a threshold voltage of 5V.

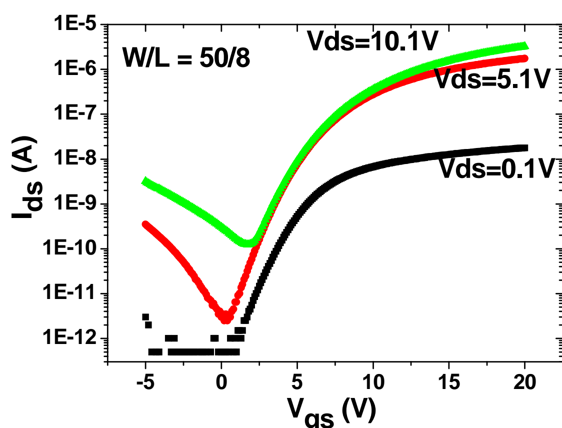
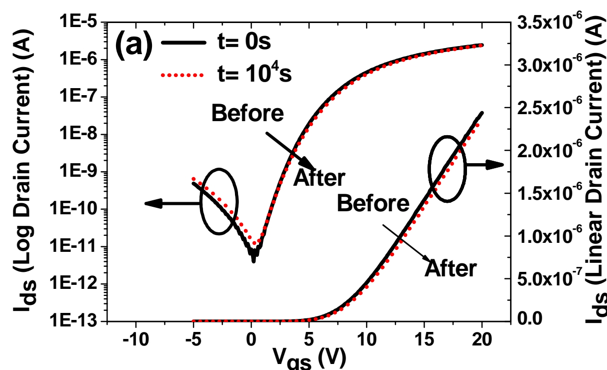


Fig. 3. Typical transfer characteristics of the DL TFT (W/L = 50 μ m/8 μ m)

Dynamic stresses are more analogous to real operating conditions than static stresses [8]. To compare the reliability of DL TFTs with that of a-Si TFTs, dynamic electrical stress analysis was performed on both transistor types. The dynamic stress conditions are listed in Table 1:

TABLE 1. Dynamic electrical stress conditions

	V_{gs} (V)	V_{ds} (V)	Frequency (Hz)	Time (sec)	Duty (%)
1	0/10	10	60K	10000	50
2	0/10	10	60, 600, 6K, 60K	10000	50
3	0/10	10	60K	10000	10, 50, 90



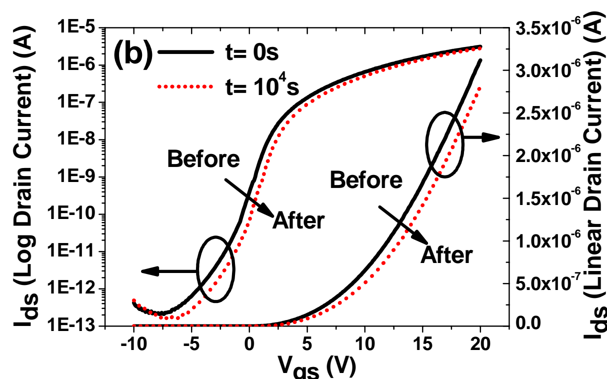


Fig. 4. Transfer characteristics of the (a) DL TFT and (b) a-Si TFT measured at V_{ds} = 5.1V under dynamic stress condition 1

Figure 4 shows the transfer characteristics of the (a) DL TFT and (b) a-Si TFT measured at V_{ds} = 5.1V under dynamic stress condition number 1 (Table 1). During real operation of the switching TFT in an AMOLED, the TFT is operated at a low frequency (~ 60Hz) and a very low duty ratio (<< 1%). We used severe stress conditions to accelerate degradation. After the application of dynamic stresses, the DL TFT showed little threshold voltage (V_{th}) shift degradation, while the a-Si TFT suffered a significant positive V_{th} shift. The degradation mechanisms of the a-Si TFT are charge trapping in the SiN_x gate insulator, and state creation in the band gap of the a-Si layer [9]. State creation is known to cause a considerable positive shift in the transfer characteristic of a-Si TFTs under positive dynamic stresses [9]. When charge trapping is dominant, a negative V_{th} shift generated under negative bias stresses occurs [9]. These results show that the DL TFT is not affected by state creation.

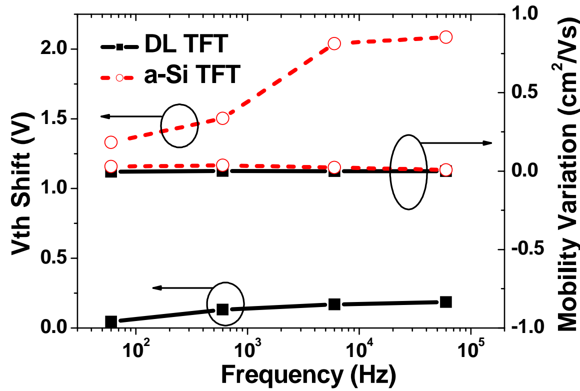


Fig. 5. The V_{th} shift and mobility variation comparison as a function of frequency in the DL TFT and the a-Si TFT, measured at V_{ds} = 5.1V under dynamic stress condition 2.

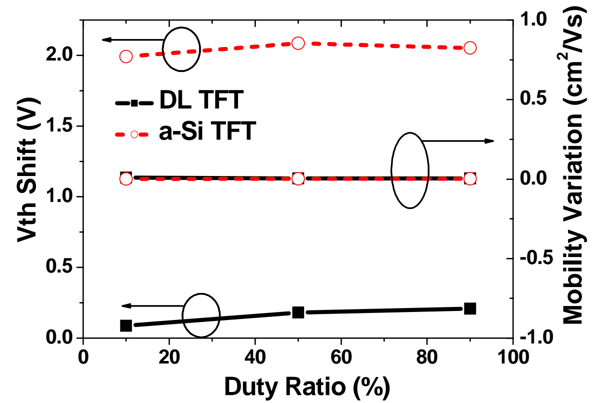


Fig. 6. The V_{th} shift and mobility variation comparison as a function of duty ratio of the DL TFT and the a-Si TFT, measured at V_{ds} = 5.1V under dynamic stress condition 3.

Figure 5 shows the V_{th} shift and mobility variation comparison of the a-Si and the DL TFTs measured at V_{ds} = 5.1V under dynamic stress condition 2 in table 1. In the a-Si TFT, the V_{th} shift increased with frequency. However, the DL TFT showed no variation in V_{th} shift. Tsujimura reported that saturation region operation of an a-Si TFT shows a smaller V_{th} shift than operation in the linear region [1]. In this experiment, both transistors showed a larger transition voltage between the linear and saturation regions as frequency was increased. In the linear region, the a-Si TFT had a larger V_{th} shift because of AC charge trapping in the gate insulator. The DL TFT showed relaxed charge injection in the linear region, maybe because of the double layer.

Figure 6 shows the V_{th} shift and mobility variation plotted against the duty ratio for the two types of transistor under stress condition 3 (Table 1), measured at 5.1V. The V_{th} shift was nearly constant in both the DL and the a-Si TFTs. This result shows that for an a-Si TFT, a pulsed transition is a greater factor in the transistor's degradation than a dynamic stress applied over time. Although the V_{th} shift in both the DL TFT and the a-Si TFT were independent of duty ratio, the DL TFT showed a smaller V_{th} shift of approximately 0.3V, while the a-Si TFT showed a V_{th} shift of approximately 2V, as seen in Figures 5 and 6. Figures 5 and 6 show that the mobility variation was unaffected by dynamic stresses. These results show that the DL TFT is more reliable than the a-Si TFT under dynamic stresses.

4. Summary

We proposed the use of DL TFTs for improved stability and production efficiency. These transistors were fabricated with a conventional bottom gate a-Si TFT process. To confirm the reliability of the device, dynamic electric stresses were applied to both a DL TFT and an a-Si TFT. The mobility variations of both transistor types under these stresses were negligible. A large positive V_{th} shift was seen in the a-Si TFT under these conditions. These results indicate that the degradation of the a-Si TFT is caused by state creation in the a-Si layer. No V_{th} shift was observed in the DL TFT. Because the channel layers of the DL TFT are made up of double layers of a-Si and μs-Si, we can conclude that the DL TFT isn't affected by state creation in the channel layers.

For the a-Si TFT, increasing the frequency produced an increased V_{th} shift, while increasing the duty ratio produced no V_{th} shift variance. From these results, we can conclude that the V_{gs} transition from the linear region to the saturation region generates more state creation than V_{gs} over time. The V_{th} shift in the DL TFT was independent of both frequency and duty ratio. In other words, the DL TFT was reliable under dynamic stress and is suitable for AMOLED applications.

5. Acknowledgements

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6. References

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