Surface Treatment Effect on Electrical Characteristics of Ink-Jet Printed Pentacene OTFTs Employing Suspended Source/Drain Electrode

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Keywords : OTFT, Surface Treatment, Ink-Jet Printing, Suspended Electrode

Abstract

The effect of gate insulator surface treatment on electrical characteristics of bottom contact (BC) and suspended source/drain (SSD) organic thin-film transistors (OTFTs) was studied. Triisopropylsilylethynyl pentacene was used as an active material and was printed by ink-jet printing method. In case of the BC OTFTs, threshold voltage was shifted from positive to near zero, and the field-effect mobility was increased when the gate insulator surface was treated with hexamethyldisilazane. However, in case of SSD OTFT, threshold voltage shift was not observed and the field-effect mobility was decreased.

1. Introduction

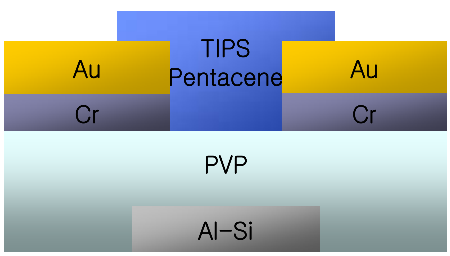
Solution-processed organic thin-film transistors (OTFTs) have attracted intensive attention due to their advantages in variable display applications such as low cost production, low temperature process and non-vacuum process. The printing method is suitable for large-area display fabrication [1][2]. However, electrical performance of solution-processed OTFTs is inferior to that of vacuum-processed OTFTs [3][4].

Commonly there are two types of the OTFT, top contact (TC) structure and bottom contact (BC) structure. The TC OTFT has higher field-effect mobility than that of the BC OTFT. It is caused by lower source/drain (S/D) contact resistance of the TC OTFT [5]. But, the channel length is limited by the feature size of a metal shadow-mask and it is hard to fabricate the channel length under 30um on large area scale [6]. In BC OTFT, it is easy to make the channel length few micro-meters by photolithography. However, the extrinsic field-effect mobility of the BC OTFT is degraded due to the high contact resistance, when the channel length is scaled down under 10um [7].

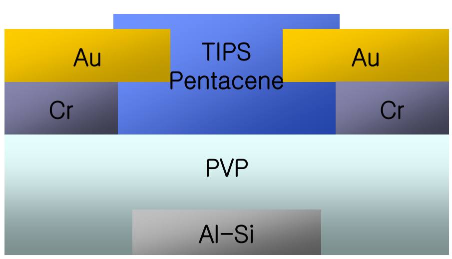
Previously we proposed a new S/D structure to improve the electric properties of OTFTs [8]. The suspended source/drain (SSD) electrodes act like as the TC electrodes, and they can be fabricated by the conventional BC OTFTs process. Moreover, it is suitable and effective structure for solution-processed OTFTs using soluble organic semiconductor. In this paper, we studied the effect of gate insulator surface treatment on electrical characteristics of BC and SSD OTFTs.

2. Experimental

The BC and SSD OTFT were fabricated by following process. A 700 um-thick glass was used as substrate. For barrier layer, 100-nm-thick silicon oxide was deposited by e-beam evaporation at elevated temperature of 110℃. On the barrier layer, 100-nm-thick Al-Si or indium-tin-oxide (ITO) was deposited for gate electrode by DC sputtering at room temperature. Then it patterned by wet etching. On the top of the gate electrode, poly-4-vinylphenol (PVP) was spin-coated. The PVP solution was 10wt% concentration, and it was mixed with poly (melamine-co-formaldehyde) methylated (5 wt%) in propylene glycol monomethyl ether acetate. The poly (melamine-co-formaldehyde) methylated was used as cross linked agent. After the PVP was coated, it was cured in a convection oven at 200℃ for 30 min. The thickness of the cured PVP was 480 nm. The PVP layer was not patterned. For S/D electrode, Cr/Au double layer was used. Cr was deposited by e-beam evaporation with 3-nm-in-thickness for the BC OTFT and 50-nm-in-thickness for the SSD OTFT. After Cr deposition, 100-nm-thick Au was deposited by thermally evaporation. Cr was used as adhesive layer for the BC and SSD OTFT. But additionally, in case of the SSD OTFT, it was used as sacrificial layer for SSD Au electrode. The suspended Au electrode was formed by completely etching the Cr layer in the active area. Figure 1 shows the structure of the BC OTFT and the SSD OTFT.



(a)



(b)

Fig. 1. Schematic structures of (a) BC OTFTs and (b) SSD OTFTs.

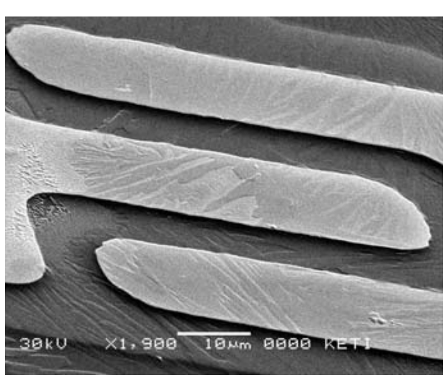
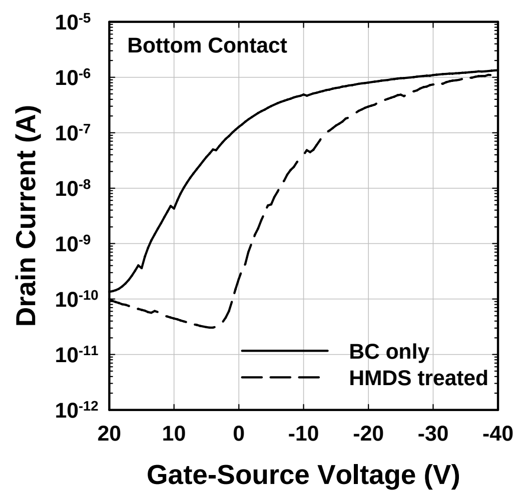


Fig. 2. Scanning electron microscopy (SEM) image of the SSD OTFT.

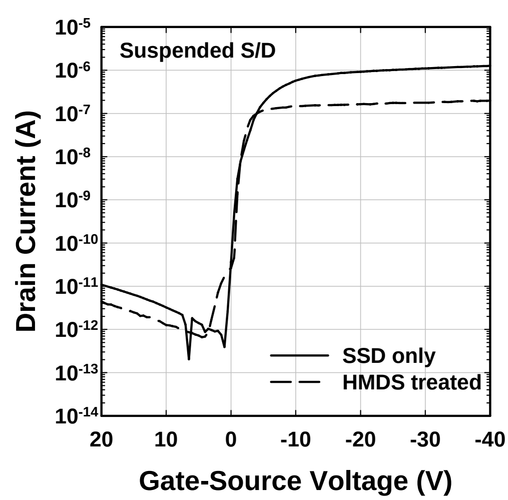
After S/D was formed, hexamethyldisilazane (HMDS) was spin coated for treatment of the gate insulator surface. Finally, triisopropylsilylethynyl (TIPS) pentacene was printed for an active layer by ink-jet printing (30 um piezo nozzle, Microfab). The TIPS pentacene ink was made of 1wt% of TIPS pentacene in anisole or chlorobenzene. Figure 2 is the SEM image of the fabricated SSD OTFT.

3. Results and discussion

Figure 3 shows the transfer characteristics of BC OTFTs with and without HMDS treatment (a) and SSD OTFTs with and without HMDS treatment (b).



(a)



(b)

Fig. 3. The transfer characteristics of (a) BC OTFT with and without HMDS treatment, (b) SSD OTFT with and without HMDS treatment.

In case of the BC OTFT, threshold voltage was shifted from +11.0 V to -3.0 V when the surface was treated. Also the field-effect mobility was increased from 0.032 cm^2/Vs to 0.041 cm^2/Vs. However, in case of HMDS treated SSD OTFT, threshold voltage was not shifted. Moreover, the field-effect mobility was decreased from 0.11 cm^2/Vs to 0.06 cm^2/Vs and the on-state current was reduced by almost one order. It can be concluded that the surface treatment by HMDS improved the performance of the BC OTFT, but it degraded the performance of the SSD OTFT. HMDS was remained within SSD electrodes and surface and made TIPS ink hard to fill under SSD electrodes. Probably the degradation was caused by the remaining HMDS between SSD electrodes and gate insulator surface.

4. Summary

We studied the gate insulator surface treatment effect on electrical characteristics of ink-jet printed TIPS pentacene OTFTs with conventional BC structures and SSD structures. The surface treatment by HMDS improved the performance of the BC OTFT, but it degraded the performance of the SSD OTFT. In case of the BC OTFTs, threshold voltage was shifted from +11 V to -3 V and the field-effect mobility was increased by the treatment. However, in case of the SSD OTFT, threshold voltage was not shifted to near zero. Moreover, the field-effect mobility was decreased from 0.11 cm^2/Vs to 0.06 cm^2/Vs and the on-state current was reduced by almost one order.

5. References

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