Degradation of High Performance Short Channel N-type Poly-Si TFT under the Electrical Bias Caused by Self-Heating

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Abstract

We have investigated degradation of short channel n-type poly-Si TFTs with LDD under high gate and drain voltage stress due to self-heating. We have found that the threshold voltage of short channel TFT is shifted to negative direction on the self-heating stress, whereas the threshold voltage of long channel is moved to positive direction.

1. Introduction

In recent days, low temperature poly-Si thin film transistors (LTPS TFTs) have attracted a considerable attention for active matrix organic light emitting diode (AMOLED) in the pixel switching and peripheral circuit [1][2]. The operation speed of pixel transistor and peripheral circuit must be higher as the resolution of display increases. The short channel poly-Si TFT is required for high resolution display due to its high current driving ability. However, the reliability of short channel poly-Si TFTs is critical issue when the channel length is decreased [3]. It has been reported that the stability of polysilicon TFTs is poor than that of single crystalline silicon MOSFETs after electrical stress [4]-[9].

The poor stability of poly-Si TFTs is due to the high density of in-grain and grain boundary defects besides interface state between the gate oxide and polysilicon film. Most previous works refer to the stability of poly-Si TFT have been focused on long channel device. However, the degradation of short channel poly-Si TFTs, especially self-heating stability, have been scarcely reported. Also degradation phenomenon of short channel Poly-Si TFT caused by the high gate and drain voltage is more originated in self-heating stress than in hot-carrier stress. Also, the self-heating effects become increasingly important as the channel length becomes smaller, especially less than 2μm.

The purpose of our work is to report the threshold voltage shift of n-channel poly-Si TFTs with short channel length under self-heating stress. The negative shift of threshold voltage is observed after high gate and drain voltage stress. This may be attributed to the holes trapping, which is generated by impact ionization, at the backside interface near the source. In order to investigate the accumulation and the trapping of holes, C-V characteristics have been measured before and after stress. Also, the holes trapping on the high temperature is verified from the negative bias temperature stress.

2. Experimental

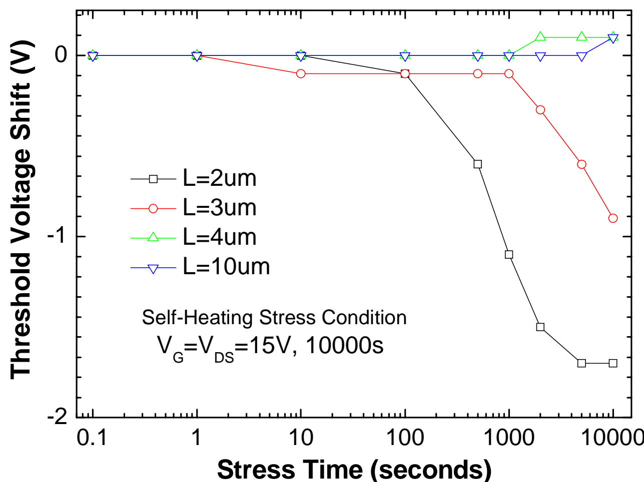
Top-gate n-channel poly-Si TFTs were fabricated using a conventional Excimer Laser Annealing (ELA). First, amorphous silicon films were deposited on the buffer oxide by Plasma Enhanced Chemical Vapor Deposition (PECVDS). Typical excimer laser annealing was utilized to crystallize the amorphous silicon film for a low temperature process followed by polysilicon active area patterning. A gate oxide (SiO_2, 80nm thick) and an interposed silicon nitride (SiN_x, 20nm thick) film were sequentially deposited in order to prevent the incorporation of mobile ions into the SiO_2 gate insulator [10]. The n+ regions were created by ion doping. A gate metal was then formed followed by doping in the lightly doped drain (LDD) region. A dielectric interlayer was deposited by PECVDS. Subsequently, dopant activation was carried out thermally. Contact holes were formed, and a source drain metal was deposited and patterned. A passivation layer was deposited and patterned to complete the fabrication process. Polysilicon TFTs used for experiment have 10 ㎛ width and 1 ㎛ LDD length. The minimum channel length is 2 ㎛. In order to investigate the stability of polysilicon TFTs under

high gate and drain voltage stress, transistor with threshold voltage about V_{TH} = 1V were subjected to electrical stress under V_{GS} = V_{DS} = 15V for 10,000 seconds.

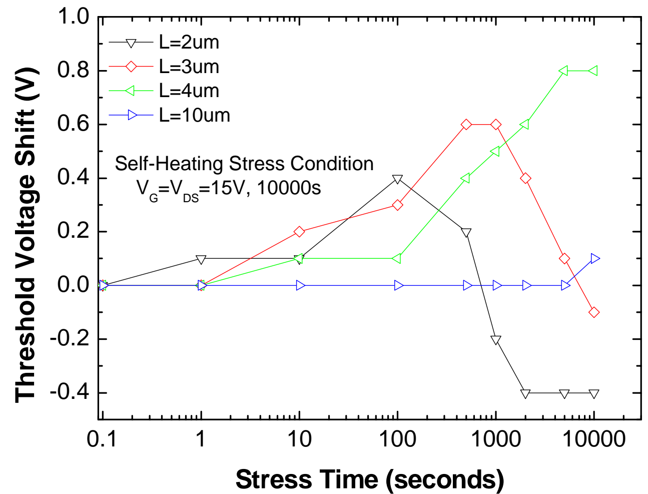
3. Results and discussion

Fig. 1 shows the threshold voltage of the polysilicon TFTs with various channel length as a function of stress time under high gate and drain voltage stress. The threshold voltages are measured at both V_{TH}=0.1V and 10V and those are defined to be the gate voltage where the drain current I_d is 100 nA × W/L for V_{TH}=10V and 10nA × W/L for V_{TH}=0.1V. The difference of the threshold voltage measured at V_{TH}=0.1V and V_{TH}=10V is induced because the electron trapping and interface state generation mainly occurs near the drain junction at front interface between polysilicon film and gate oxide. The threshold voltage measured at V_{TH}=10V is relatively less affected by the damaged drain region. Under the high gate and drain voltage stress, the negative shift of threshold voltage measured at V_{TH}=10V becomes large as channel length is shorter.

In poly-Si TFT with channel length 2 ㎛, the threshold voltage measured at V_{TH}=0.1V, at first, is increased due to the generation of the trap state near the drain junction. After some stress time goes, the threshold voltage is decreased so that it moves under the initial threshold voltage after 10,000 seconds. While, the threshold voltage measure at V_{TH}=10V is decreased for whole stress time.



(a)



(b)

Fig. 1. Variation of threshold voltage of the poly-Si TFT with various channel length as a function of stress time under the stress condition V_G= V_{TH} = 15V, measured in (a) V_{TH}=0.1V and (b) V_{TH}=10V.

It is suggested that trap states generation at front interface (between polysilicon film and gate oxide) and hole trapping at backside interface (between buffer oxide and polysilicon film) on the high temperature simultaneously occur. It is reported that device temperature under high gate and drain voltage stress condition can be increased above 200 °C. [11]

In order to investigate the phenomena, C-V measurement is performed in the short channel poly-Si TFTs before and after high gate and drain voltage stress. Fig. 2 shows the C_{GD} and C_{GS} before and after the stress (V_G = V_{TH} = 15V). The C_{GD} curve is shifted to negative direction and slightly stretched out. While, the C_{GS} curve is more shifted to negative direction and considerably stretched out. The negative shift of curves after the stress may be due to the hole trapping at the back interface. The stretched-out of curves means that the amount of holes trapping is larger in the region which is closer to the source. The holes generated by impact ionization near the drain junction is migrated from drain to source along the backside interface because of the lowest potential for holes so that the holes are accumulated and trapped at backside interface near the source. The holes trapped at backside interface increase the body potential so that the negative shift of C-V curves is induced.

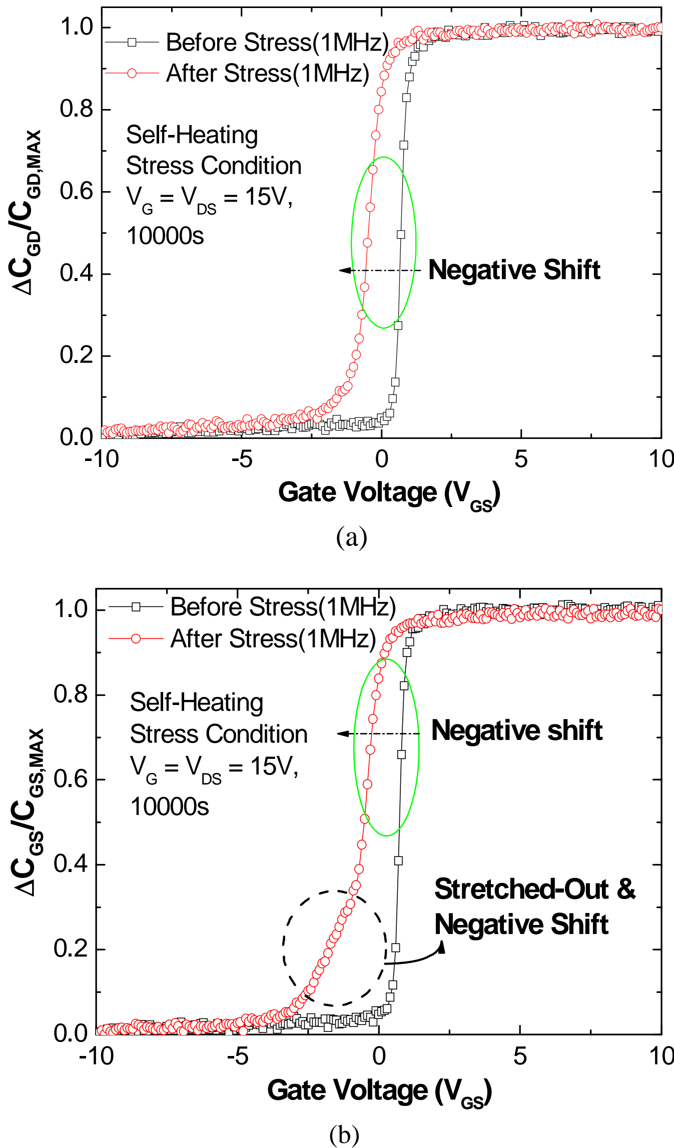


Fig. 2. (a) Gate-to-Drain capacitance and (b) Gate to-Source capacitance of the poly-Si TFT before and after stress $V_G = V_{TH} = 15V$ for 10,000 seconds, measured at 1MHz.

In order to investigate the holes trapping at the interface, we have applied the negative bias temperature stress: $V_G = -5V$, $V_S = V_{TH} = 0V$ at 240°C for 10000 seconds. Gate bias ($V_G = -5V$) is applied for enough inducing the hole accumulation at front interface. In our experiment, negative bias temperature stress under 200°C cannot change the electrical characteristics, especially threshold voltage. Fig. 3 shows the results before and after bias temperature stress of polysilicon TFTs at 240 °C. The results show that the hole accumulated at backside interface can be trapped into the buffer oxide at high temperature. It is well-know that backside interface between polysilicon layer and buffer oxide has more interface defect density than front interface between gate oxide and polysilicon layer [12]. Experiment condition in Fig. 3 can induce more holes trapping at backside interface. Therefore, the holes trapping at backside interface near the source and trap states generation at front interface near the drain affect the electrical characteristics under self-heating stress, as shown in Fig. 4.

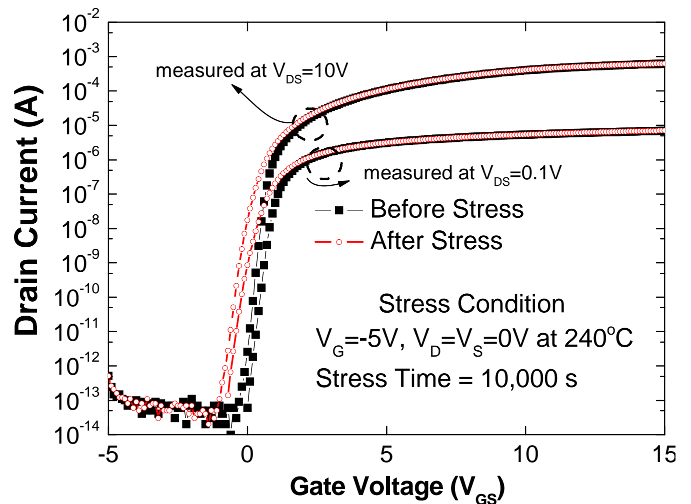


Fig. 3. Transfer characteristics of n-channel polysilicon TFTs before and after stress at $V_G = -5V$, $V_S = V_{TH} = 0V$ at 240 °C, measured at $V_{TH} = 0.1V$ and $V_{TH} = 10V$.

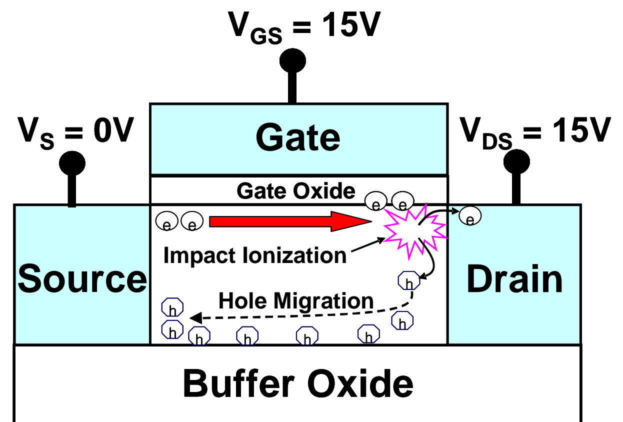


Fig.4. Schematic diagram of poly-Si TFT's degradation under the self-heating stress

4. Summary

We have investigated the stability of short channel n-type polysilicon TFTs with LDD under the self-heating stress. Threshold voltage measured at high drain voltage, which is relatively less affected damaged region near the drain junction, is moved to negative direction. This can be attributed to the hole trapping at the backside interface near the source. C-V measurements verify the suggestion that the holes trapping occurs at backside interface near the source. The C_{GD} curves are shifted in negative direction and slightly stretched out. While, the C_{GS} curves are more shifted in negative direction and considerably stretched out. The negative shift of curves after the stress may be due to the hole trapping at the back interface. The stretched-out of curves means that the amount of the holes trapping is larger close to source region. Negative bias temperature stress shows that the holes can be trapped at back interface on the high temperature.

5. References

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