

Characteristics of MINOS Structure using TiO₂ as Blocking Layer for Nonvolatile Memory applicable to OLED

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Abstract

Titanium dioxide (TiO₂) is promising candidate for fabricating blocking layer of gate dielectrics in non-volatile memory (NVM). In this work, we investigated TiO₂ as high dielectric constant material instead of silicon dioxide (SiO₂), which is generally used as blocking layer for NVM.

1. Introduction

Active-matrix organic light emitting diode (AMOLED) displays have been considered a potential candidate for the next generation of flat panel displays due to the ability of AMOLED in providing wider viewing angle, superb display image quality, and lower fabrication cost compare to the active matrix liquid crystal displays (AMLCDs)[1-2]. However, AMOLED have the non-uniformity of brightness and panel problem. Since device aging, temperature and fabrication processes cause variations in the characteristics of AMOLED, NVM is capable of compensating the variations and produce the desired brightness uniformity[3-4].

NVM can retain the stored information even when not powered. Metal-Oxide-Nitride-Oxide-Semiconductor (MONOS) of NVM's structure have attracted much attention in the semiconductor industry due to their advantages including lower programming voltage, better scalability, improved endurance and a simple fabrication process compatible with standard CMOS technology[5].

Aggressive scaling down of gate length and gate blocking oxide thickness in NVM for high performance and circuit density aggravates the problems of high gate leakage current, standby power consumption and gate oxide reliability. Below the

physical thickness of 15 Å, the gate leakage current exceeds the specifications (1 A/cm²). To address these issues, recently there has been much interest in high dielectric constant (high-k) materials as the potential gate dielectrics because of low gate leakage current. High-k gate dielectrics such as aluminium oxide (Al₂O₃ : k~10), hafnium dioxide (HfO₂ : k~25), zirconium dioxide (ZrO₂ : k~25), lanthanum oxide (La₂O₃ : k~27) and titanium dioxide (TiO₂ : k~40) have received much attention recently for use gate dielectrics. TiO₂ is promising candidate for fabricating blocking layer of gate dielectrics in NVM without the problem of conventional SiO₂ because of its high dielectric constant[6-10].

In this paper, TiO₂ is utilized as the blocking layer to prevent carriers injecting from the gate electrode.

2. Experimental

The wafers used in this study were boron-doped p-type (100) silicon substrate with resistivities of 1~10Ω-cm. The wafers were cleaned immediately before TiO₂ deposition with a 30 second immersion in buffered HF (10% HF), followed by a 120 second rinse in deionized water to eliminate native oxide layer. After cleaning, the wafers were inserted into the deposition chamber of atmospheric pressure chemical vapor deposition (APCVD) system and heated to the desired deposition temperature. The TiO₂ film was deposited by varying the temperature from 200°C to 300°C and keeping the deposition thickness fixed at approximately 120 Å. The organic precursor titanium tetraisopropoxide [(OC₃H₇)₄Ti, TTIP] was kept in a bubbler that was maintained at 60°C include flow rates of gases and deposition time. All the samples

deposited at different temperatures were then subjected to X-ray diffraction (XRD), optical properties and ellipsometry measurements in which the thickness and the refractive index of each sample were determined by using ellipsometry. A metal-insulator-semiconductor (MIS) structure device was then fabricated using all the films in order to study their electrical properties. For the fabrication of the MIS device, a high-vacuum thermal evaporator was used to deposit metal dots of aluminum as the electrode. The capacitance-voltage (C-V) characteristics of the MIS devices were analyzed using standard software of materials development corporation advanced semiconductor analysis program.

To study the effect of charge storage, p-type (100) silicon substrates were used for the fabrication of metal-insulator(TiO_2)-nitride-oxide-semiconductor (MINOS) devices. After cleaning with conventional procedure the wafer was immediately transferred into the chamber for plasma treatment. The SiO_xN_y layers were created by nitrous oxide (N_2O) plasma exposure under radio frequency (RF) powers of 150W by inductively coupled plasma chemical vapor deposition. During plasma treatment, N_2O flow rate was maintained to be 2.5 sccm and the working pressure in the discharge chamber was 8.8 mTorr. The silicon nitride (SiN_x) was deposited to use as a charge trap region on silicon oxynitride (SiO_xN_y) layer and the TiO_2 was deposited to act as a blocking oxide layer on SiN_x film. Schematic view of MINOS structure for NVM on glass is shown in Fig. 1.

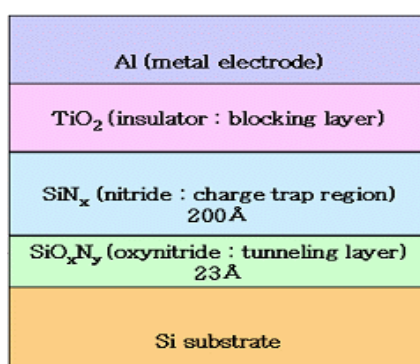


Fig. 1. Cross sectional view of MINOS structure.

3. Results and discussion

For investigating properties of TiO_2 films deposited with TTIP by using APCVD, substrate temperature was changed from 200 °C to 300 °C at an interval

of 50 °C under O_2 flow rate of 5 lpm, N_2 flow rate of 5 lpm and bubbler temperature of 60 °C. The thickness of the deposited TiO_2 films was fixed as 120 Å. The variation of film thickness and refractive index with substrate temperature are shown in Fig. 2. It can be seen clearly from the figure 2 that the refractive index increases linearly as the substrate temperature rises whereas film thickness was found to be almost constant with substrate temperature.

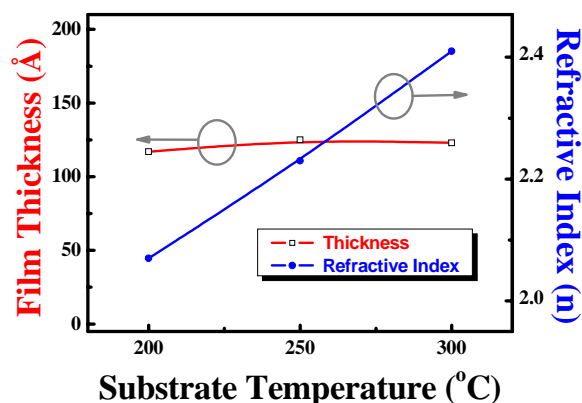


Fig. 2. Variation of film thickness and the refractive index with the substrate temperature during deposition.

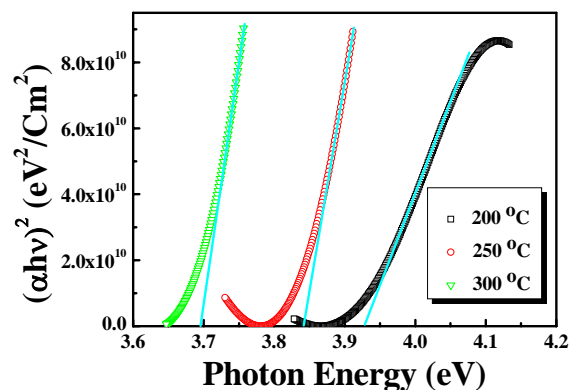


Fig. 3. Square of the absorption coefficient vs the photon energy for TiO_2 films.

The absorption coefficient of the films has been calculated using optical transmittance and calculation. The optical band gap of the TiO_2 films was

determined by extrapolating of the linear part of the spectral dependence $(\alpha h\nu)^2$ vs. $h\nu$ to the photon energy axis, Fig. 3. It is clear seen from Fig. 4 that the fundamental absorption edge shifts to higher energy with decreasing deposition temperature ($E_g \sim 3.7, 3.83$ and 3.93 eV for $300, 250$ and 200 °C, respectively). So, the estimated optical band gap in our TiO_2 films decreases in the range of $3.93 - 3.7$ eV, depending on growth temperature.

Fig. 4. shows the XRD analyses of the four samples in the 200°C , 250°C , 300°C and bare-Si wafer. The TiO_2 film deposited at substrate temperature of 200°C , 250°C , 300°C showed some additional peaks in the direction (101) and (200) pertaining to the 25.2 and 48 degree at the positions corresponding to the anatase type structure of the TiO_2 .

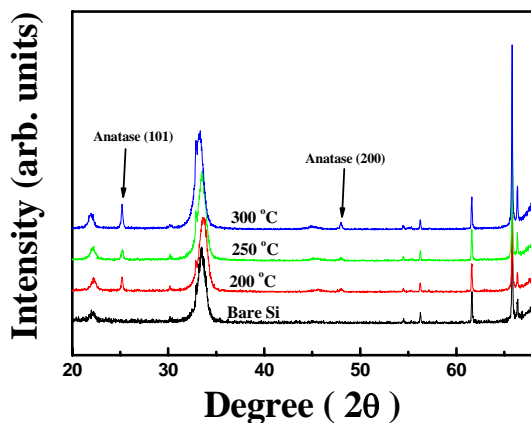


Fig. 4. XRD of TiO_2 films with the substrate temperature during deposition.

The characteristic C-V curves of MIS structure fabricated by using TiO_2 formed at different substrate temperature as insulator layer are shown in Fig 5. The C-V curve for the TiO_2 film grown at high substrate temperature is the good curve. This result may be caused by the increase in the positively fixed charge density with the decrease in the substrate temperature for deposition of TiO_2 thin film. It is also seen that the slope of the C-V curve between the accumulation and inversion region decreases with the decrease in the substrate temperature for deposition of TiO_2 thin film. The increase in the stretch out of the C-V curves is caused by an increase in the interface trap density with the decrease in the substrate temperature. TiO_2

thin film deposited by employing substrate temperature of 300 °C shows the least mobile charge and clear separation between inversion and accumulation regions.

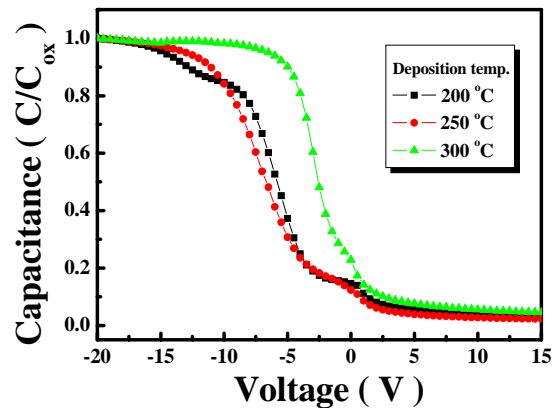


Fig. 5. C-V characteristics of the MIS structures with TiO_2 insulator formed at different substrate temperature.

MONOS and MINOS memory devices were fabricated for the verification of the functioning of SiO_2 and TiO_2 as blocking layers. When the MONOS memory device was fabricated, the SiO_xN_y film of 23 Å thickness was used as tunneling layer, SiN_x with thickness of 360 Å was used as charge trap region on SiO_xN_y film, and SiO_2 with thickness of 120 Å was used as blocking layer on SiN_x film. When the MINOS memory device was fabricated, tunneling layer of SiO_xN_y and charge trap region of SiN_x were deposited with the same thickness as in case of MONOS memory device whereas TiO_2 with refractive index of 2.6 and thickness of 120 Å was used as blocking layer instead of SiO_2 . The characteristic C-V curves exhibiting the memory properties of the fabricated MONOS and MINOS memory devices are shown in Fig. 6. The C-V characteristic curve of MONOS and MINOS device showed that the width of C-V hysteresis is in the large range voltage sweeps from -10V to $+10\text{V}$. The sweep direction of MONOS devices with SiO_2 layers as blocking layer thickness of 120 Å and MINOS devices with TiO_2 layers as blocking layer thickness of 120 Å is clockwise due to the charge injection and erasing from channel. C-V characteristic curve of MONOS and MINOS devices showed the width of the C-V hysteresis was 1 V and

2.3 V in the large range voltage sweeps ranging from -10V to +10V due to the charge storage effect. From the C-V characteristic curves in Fig. 6, the relatively large ΔV_{FB} of 2.3 V is shown in MINOS device using TiO_2 as blocking layer, compared to ΔV_{FB} of 1.3 V of MONOS device using SiO_2 as blocking layer, which can be attributed to the high trap density in the charge trap region of SiN_x and efficient blocking function of TiO_2 thin film.

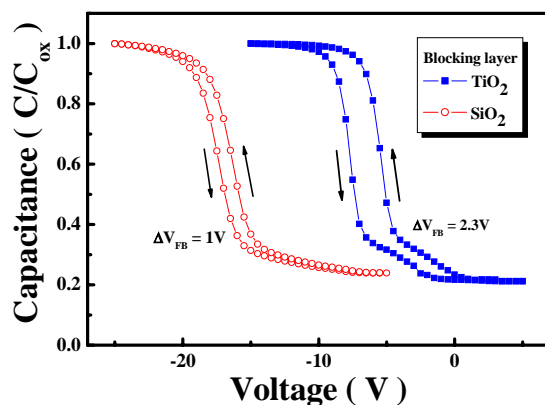


Fig. 6. C-V hysteresis of MONOS and MINOS memory devices.

4. Summary

In this paper, we studied TiO_2 as high-k material instead of conventional SiO_2 , which is generally used as blocking oxide for NVM on glass. The characteristics of TiO_2 films deposited by using APCVD as blocking layers for fabrication of low temperature NVM on glass were investigated. The MIS structures using TiO_2 film as insulator layer were fabricated. The MINOS device using SiO_xN_y with thickness of 23 Å as tunneling layer, SiN_x with thickness of 360 Å as charge trap region, and TiO_2 with thickness of 120 Å as blocking layer were fabricated for investigation of TiO_2 thin film as blocking layer. The relatively large ΔV_{FB} is shown in MINOS device using TiO_2 as blocking layer, compared to ΔV_{FB} in MONOS device using SiO_2 as blocking layer, which can be attributed to the high trap density in the charge trap region of SiN_x and efficient blocking function of TiO_2 thin film. The TiO_2 thin film reported in this paper can be used for enhancement of charge storage of NVM on glass.

5. References

1. A. Nathan, G.R. Chaji, and S.J. Ashtiani, *IEEE J. of Display Technology*, 1, p. 267-277, (2005).
2. M. Hack, J.J. Brown, J.K. Mahon, R.C. Kwong, and R. Hewitt, *J. of the SID*, 9, p. 191-195, an (2001).
3. Hau-Yan Lu, Po-Tsun Liu, Ting-Chang Chang, and Sien Chi, *IEEE Electron Device Letters*, 27, 9, (2006).
4. Yen-Chung Lin, Member and Han-Ping D. Shieh, *IEEE Electron Device Letters*, 25, 11, (2004).
5. Yijie Zhao, Xiaonan Wang, Huiling Shang, Marvin H. White, *Solid-State Electronics*, 50, p. 1667-1669, (2006).
6. G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, *IEEE Transactions on Device and Materials Reliability*, 5, 1, (2005).
7. N. R. Mohapatra, M. P. Desai, S. G. Narendra and V. R. Rao, *IEEE Transactions on Electron Devices*, 49, 5, (2002).
8. J. Yan, D. C. Gilmer, S. A. Campbell, W. L. Gladfelter and R. G. Schmid, *J. Vac. Sci. & Technol.*, B14, p. 1706-1711, (1996).
9. Y. H. Do, K. W. Jeong, C. O. Kim and J. P. Hong, *Journal of the Korean Physical Society*, 48, 6, p. 1492-1495, (2006).
10. S. W. Jeong, K. S. Kim, M. T. You, Y. Roh, T. Noguchi, J. Jung and J. Y. Kwon, *Journal of the Korean Physical Society*, 47, S401-S403, (2005).